NSI1042/NSI1052
Isolated CAN Transceiver

Datasheet (EN) 1.3

Product Overview

The NSI1042 is an isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSI1042 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSI1042 device is safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSI1042 is up to 5Mbps. The NSI1042 provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- Up to 5000Vrms Insulation voltage
- Power supply voltage

  VDD1: 2.5V to 5.5V

  VDD2: 4.5V to 5.5V
- Bus fault protection of -70V to +70V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Data rate: up to 5Mbps
- Ideal Passive, High Impedance Bus and Logic Terminals When Unpowered
- High CMTI: 150kV/us
- Low loop delay: <220ns
- High system level EMC performance:

  Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:

  SOW8

  SOW16

Safety Regulatory Approvals

- UL recognition: up to 5000Vrms for 1 minute per UL1577
- CQC certification per GB4943.1-2022
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated CAN Bus
- Telecom

Device Information

Part Number	Package	Body Size
NSI1042-DSWVR	SOW8	5.85mm ×7.50mm
NSI1042-DSWR	SOW16	10.30mm × 7.50mm
NSI1052-DSWR	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

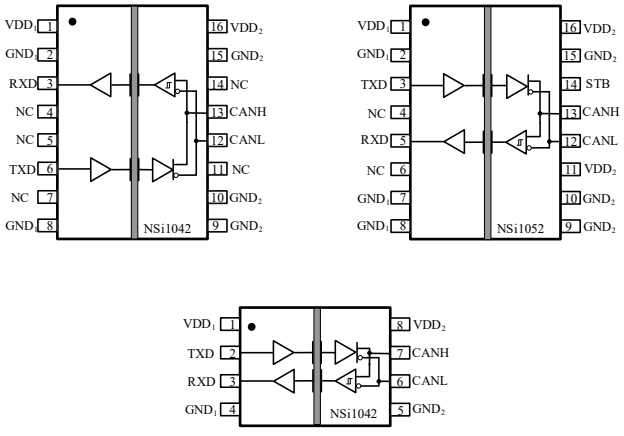


Figure 1. NSI1042 Block Diagram

INDEX

1. Pin Configuration and Functions

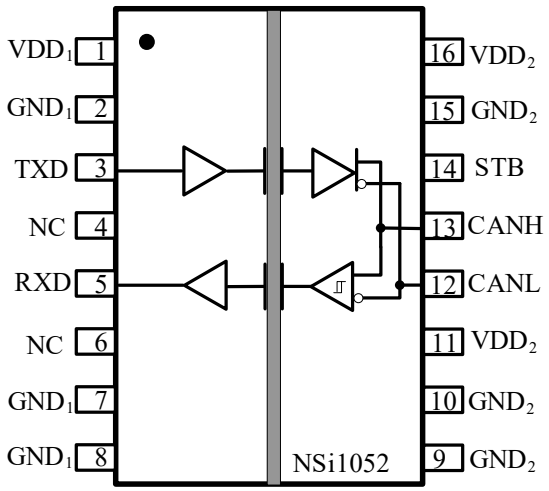


Figure 1.1 NSI1052-DSWR Package

Table 1.1 NSI1052-DSWR Pin Configuration and Description

NSI1052-DSWR PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD_1	Power Supply for Side 1
2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
4	NC	No Connection
5	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
6	NC	No Connection
7	GND_1	Ground 1, the ground reference for Isolator Side 1
8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Bus Side
10	GND_2	Ground 2, the ground reference for Isolator Bus Side
11	VDD_2	Power supply for Bus Side, this pin must be connected externally to PIN16
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	STB	Standby mode control input
15	GND_2	Ground 2, the ground reference for Isolator Bus Side
16	VDD_2	Power supply for Bus Side, this pin must be connected externally to PIN11

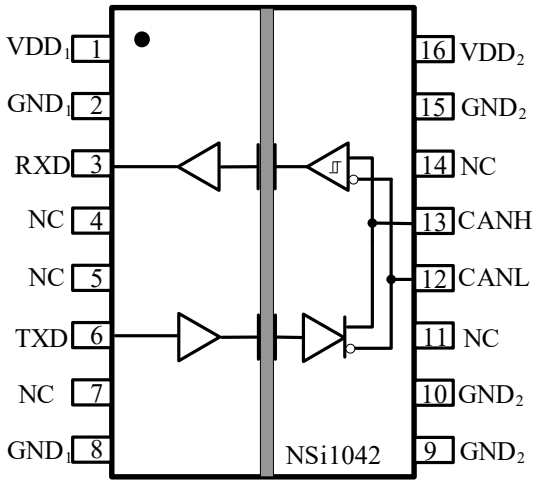


Figure 1.2 NSI1042-DSWR Package

Table 1.2 NSI1042-DSWR Pin Configuration and Description

NSI1042-DSWR PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD_1	Power Supply for Side 1
2	GND_1	Ground 1, the ground reference for Isolator Side 1
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	NC	No Connection
5	NC	No Connection
6	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
7	NC	No Connection
8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Bus Side
10	GND_2	Ground 2, the ground reference for Isolator Bus Side
11	NC	No Connection
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	NC	No Connection
15	GND_2	Ground 2, the ground reference for Isolator Bus Side
16	VDD_2	Power supply for Bus Side

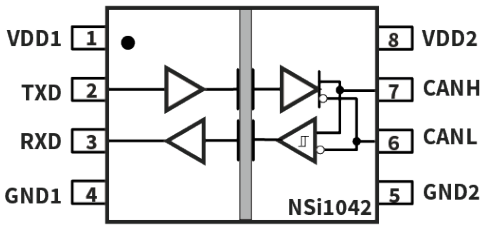


Figure 1.3 NSI1042-DSWVR Package

Table 1.3 NSI1042-DSWVR Pin Configuration and Description

NSI1042-DSWVR PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD_1	Power Supply for Side 1
2	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	GND_1	Ground 1, the ground reference for Isolator Side 1
5	GND_2	Ground 2, the ground reference for Isolator Bus Side
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	VDD_2	Power supply for Bus Side

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD_1, VDD_2	-0.5		6.5	V	
Maximum Input Voltage	V_{TXD}	-0.4		VDD_1+0.4	V	
Maximum BUS Pin Voltage	V_{CANH}, V_{CANL}	-70		+70	V	
Output current	I_o	-15		15	mA	
Operating Temperature	T_{opr}	-40		125	℃	
Storage Temperature	T_{stg}	-65		150	℃	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply voltage, controller side	V_{CC1}	2.5		5.5	V	
Supply voltage, bus side	V_{CC2}	4.5	5	5.5	V	
Voltage at bus pins (separately or common mode)	V_I or V_{IC}	-30		30	V	
High-level input voltage	V_{IH}	2		5.5	V	TXD
Low-level input voltage	V_{IL}	0		0.8	V	TXD
High-level output current	I_{OH}	-70			mA	Driver
		-4			mA	Receiver
Low-level output current	I_{OL}			70	mA	Driver
				4	mA	Receiver
Ambient Temperature	T_A	-40		125	℃	
Junction temperature	T_J	-40		150	℃	

4. Thermal Information

Parameters	*Symbol*	*SOW8*	*SOW16*	*Unit*
Junction-to-ambient thermal resistance	θ_{JA}	100	69.9	℃/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	40.8	31.8	
Junction-to-board thermal resistance	θ_{JB}	51.8	29	

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, T_A =-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 5V, T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Voltage	VDD_1	2.5		5.5	V	
	VDD_2	4.5	5	5.5	V	
Logic side supply current	IDD_1		1.97	3.50	mA	VDD_1=3.3V, TXD=0
			0.97	2.00	mA	VDD_1=3.3V, TXD=VCC1
			2.02	3.50	mA	VDD_1=5V, TXD=0
			1.02	2.00	mA	VDD_1=5V, TXD=VCC1
Bus side supply current	IDD_2		46	70	mA	VI=0V, R_{Load}=60Ω
			4.45	10	mA	VI=VDD_2
Thermal-Shutdown Threshold	T_{TS}	155	165	180	℃	
Common Mode Transient Immunity	CMTI	±100	±150		kV/us	
Logic Side						
High level input voltage	V_{IH}	2			V	TXD pin
Low level input voltage	V_{IL}			0.8	V	TXD pin
High level input current	I_{IH}			10	uA	TXD pin
Low level input current	I_{IL}	-10			uA	TXD pin
Output Voltage High	V_{OH}	VDD_1-0.4			V	I_{OH} = -4mA, RXD pin
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 4mA, RXD pin
Input Capacitance	C_{IN}		2		pF	TXD pin
Driver						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.8	3.44	4.5	V	TXD=0V, R_{Load}=60Ω
CANL output voltage (Dominant)	$V_{OL(D)}$	0.8	1.33	2.25	V	TXD=0V, R_{Load}=60Ω
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	0.5*VDD2	3	V	TXD=VDD1, R_{Load}=60Ω
Differential output voltage (Dominant)	$V_{OD(D)}$	1.5		3	V	VCC=5V, TXD=0, R_{Load}=60Ω, see Figure 5.1

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Differential output voltage (Recessive)	$V_{OD(R)}$	-0.05		0.05	V	VCC=5V, TXD=VIO, R_{Load}=60Ω, see Figure 5.1
		-0.1		0.1	V	VCC=5V, TXD=V_{IO}, NO Load, see Figure 5.1
Dominant short-circuit output current	$I_{O(sc)dom}$	-100		-40	mA	TXD=0V, t < $t_{to(dom)TXD}$, V_{CANH}=-30V
		40		100	mA	TXD=0V, t < $t_{to(dom)TXD}$, V_{CANL}=30V
Recessive short-circuit output current	$I_{O(sc)rec}$	-5		5	mA	Normal/Silent mode; V_{TXD} = VDD1. V_{CANH} = V_{CANL} = -27 V to +30 V
Receiver						
Positive-going bus input threshold voltage	V_{IT+}		750	900	mV	-12V<V_{COM}<+12V
Negative-going bus input threshold voltage	V_{IT-}	500	650		mV	
Hysteresis voltage	V_{HYS}		100		mV	
Power-off (unpowered) bus input leakage current	$I_{IOFF(LKG)}$	-5		5	uA	V_{CANH} /V_{CANL} = 5V, VCC = 0V, VIO= 0V
Input capacitance to ground	C_I		13		pF	CANH or CANL
Differential input	C_{ID}		5		pF	
Differential input resistance	R_{ID}	19	33	52	kΩ	-2V ≤ VCANH ≤ 7V, -2V ≤VCANL ≤ 7V, RID=RCANH+RCANL
Input resistance	R_{IN}	9	16	28	kΩ	-2V ≤ VCANH ≤ 7V, -2V ≤VCANL ≤ 7V
Input resistance matching	RI_{match}	-3		+3	%	CANH=CANL
Common-mode voltage range	V_{COM}	-30		+30	V	

5.2. Switching Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, T_A =-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 5V, T_A = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Loop delay1	T_{loop1}		120	220	ns	Driver input to receiver output, Recessive to Dominant, see Figure 5.7
Loop delay2	T_{loop2}		100	220	ns	Driver input to receiver output, Dominant to Recessive, see Figure 5.7
transmitted recessive bit width	$t_{bit(bus)}$	435		530	ns	$t_{bit(TXD)}$ = 500 ns
		155		210	ns	$t_{bit(TXD)}$ = 200 ns
bit time on pin RXD	$t_{bit(RXD)}$	400		550	ns	$t_{bit(TXD)}$ = 500 ns
		120		220	ns	$t_{bit(TXD)}$ = 200 ns
Driver						
Propagation delay time, recessive -to- dominant output	t_{PLH}		100		ns	see Figure 5.4
Propagation delay time, dominant -to- recessive output	t_{PHL}		80		ns	see Figure 5.4
Differential output signal rise time	t_r		42		ns	see Figure 5.4
Differential output signal fall time	t_f		32		ns	see Figure 5.4
Bus dominant time-out time	t_{TXD_DTO}	800	2000	4000	us	see Figure 5.8
Receiver						
Propagation delay time, low-to-high-level output	t_{PLH}		50		ns	see Figure 5.6
Propagation delay time, high-to-low-level output	t_{PHL}		30		ns	see Figure 5.6
RXD signal rise time	t_r		3		ns	see Figure 5.6
RXD signal fall time	t_f		3		ns	see Figure 5.6

5.3. Parameter Measurement Information

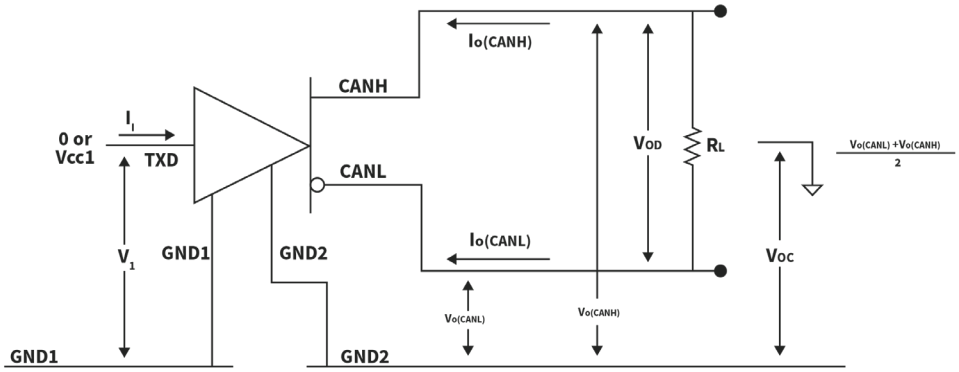


Figure 5.1. Driver Voltage, Current and Test Definitions

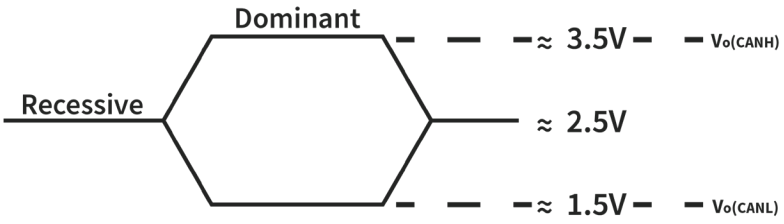


Figure 5.2. Bus Logic State Voltage Definitions

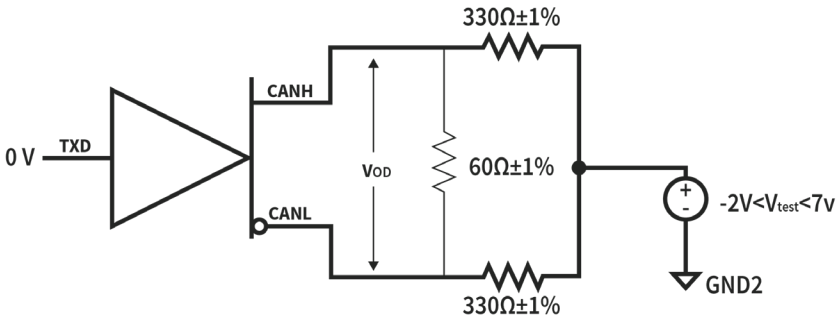
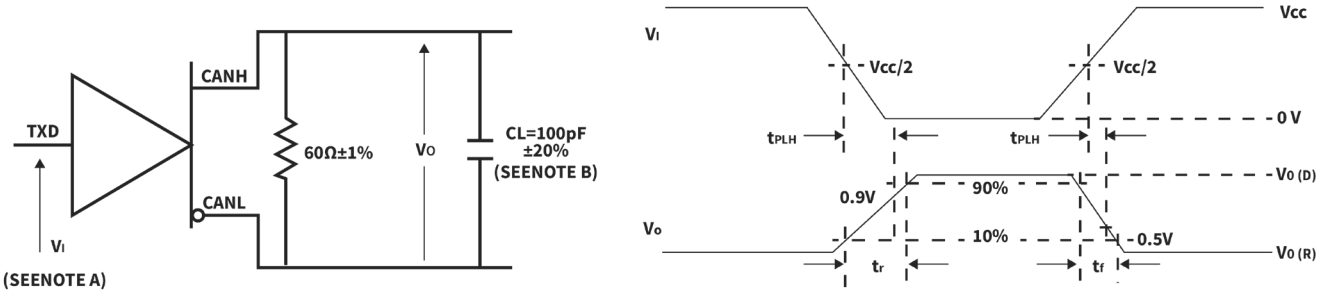


Figure 5.3. Driver VOD With Common-Mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, ZO = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 5.4. Driver Test Circuit and Voltage Waveform

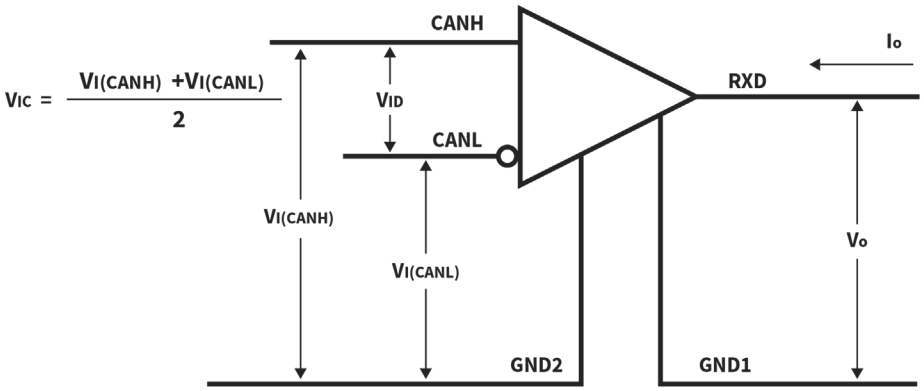
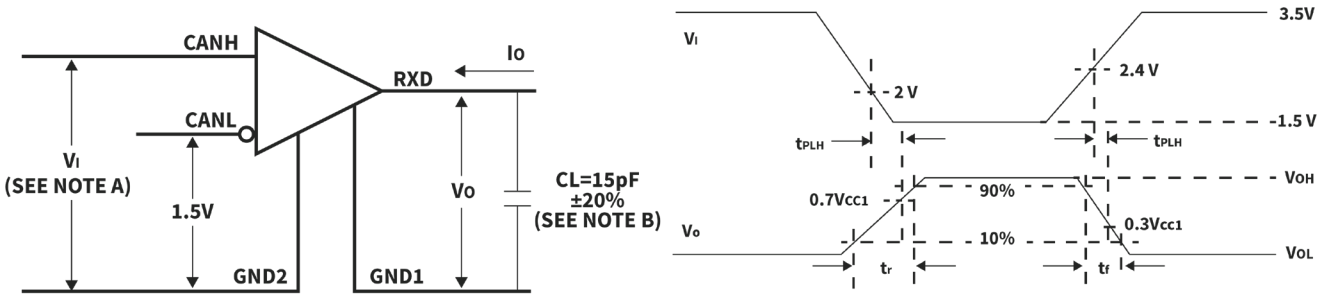


Figure 5.5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.6. Receiver Test Circuit and Voltage Waveform

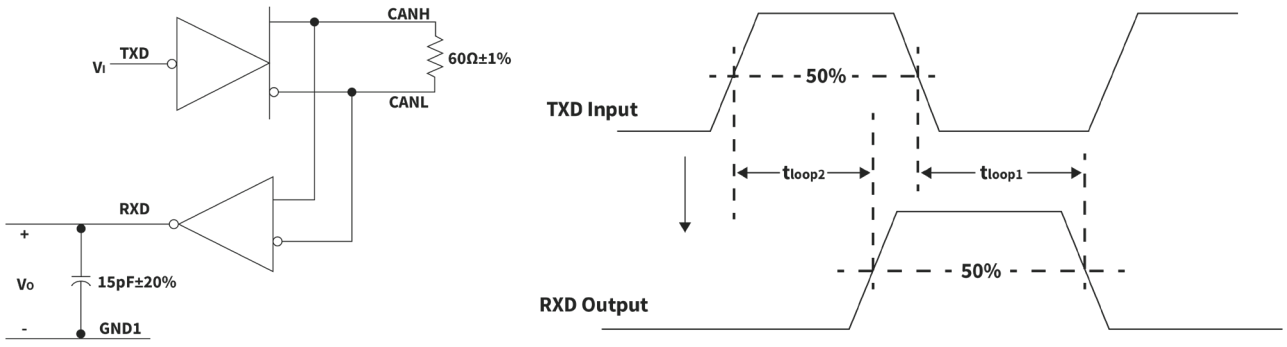
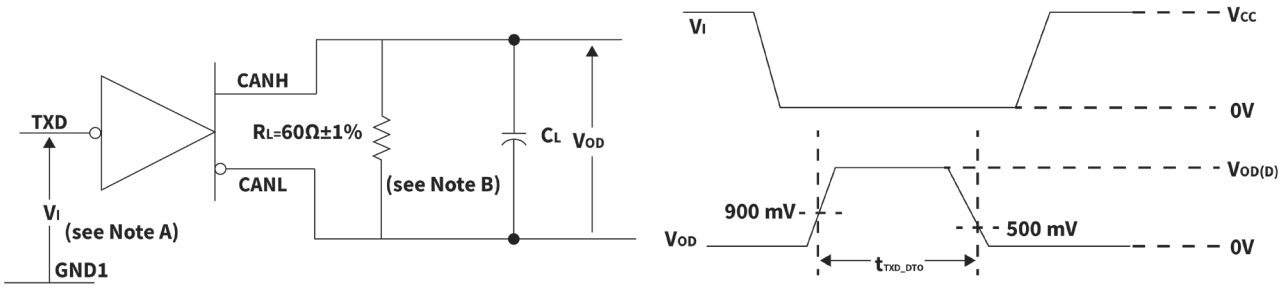


Figure 5.7. t_{LOOP} Test Circuit and Voltage Waveform



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.8. Dominant Time-out Test Circuit and Voltage Waveform

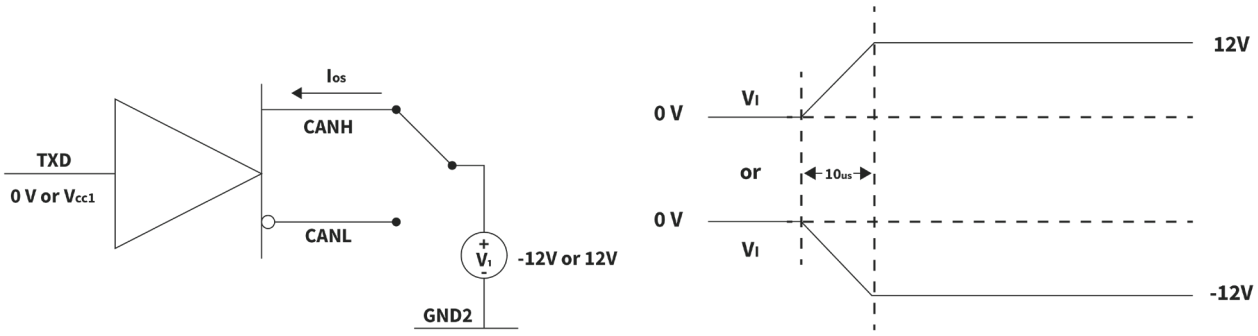


Figure 5.9. Driver Short-Circuit Current Test Circuit and Waveform

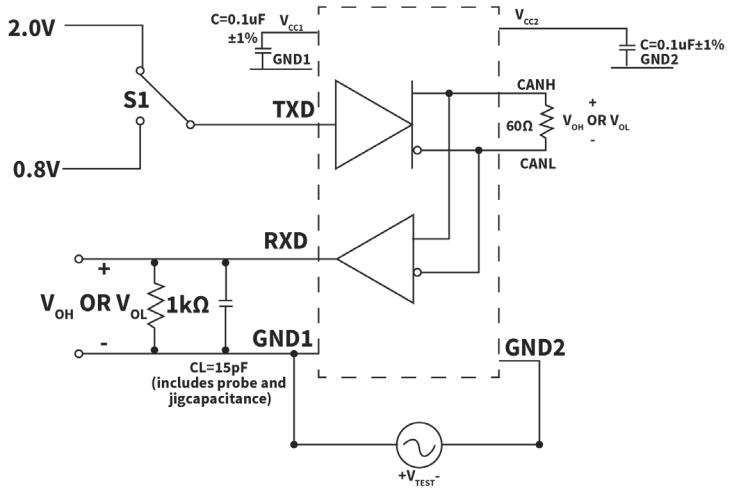


Figure 5.10. Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Description	Test Condition	Symbol	Value		Unit
			SOW8	SOW16	
Min. External Air Gap (Clearance)		CLR	8	8	mm
Min. External Tracking (Creepage)		CPG	8	8	mm
Distance through the Insulation		DTI	28		um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600		V
Material Group	IEC 60112		I		
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ≤ 150Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 600Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 1000Vrms			I to III	I to III	
Insulation Specification per DIN EN IEC 60747-17 (VDE 0884-17):2021-10[1)]					
Climatic Category			40/125/21		
Pollution Degree	per DIN VDE 0110, Table 1		2		
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	1500	V_{RMS}
	DC voltage		2121	2121	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	2121	2121	V_{peak}
Input to Output Test Voltage, Method B1	$V_{ini.b} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.875$, $t_{ini} = t_m = 1$ sec, $q_{pd} \leq 5$ pC, 100% production test	$V_{pd(m)}$	3977	3977	V_{peak}
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{ini.a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.6$, $t_{ini} = 60$ sec, $t_m = 10$ sec, $q_{pd} \leq 5$ pC	$V_{pd(m)}$	3394	3394	V_{peak}
Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{ini.a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.2$, $t_{ini} = 60$ sec, $t_m = 10$ sec, $q_{pd} \leq 5$ pC	$V_{pd(m)}$	2545	2545	V_{peak}
Maximum Transient Isolation Voltage	t = 60 sec	V_{IOTM}	8000	8000	V_{peak}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$	V_{IOSM}	6250	6250	V_{peak}

Description	Test Condition	Symbol	Value		Unit
Isolation Resistance	V_{IO} = 500 V, $T_A = T_S$	R_{IO}	>10^9		Ω
	V_{IO} = 500 V, 100 °C ≤T_A ≤ 125 °C		>10^{11}		Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1.2		pF
Insulation Specification per UL1577					
Withstand Isolation Voltage	V_{TEST} = 1.2 × V_{ISO}, t = 1 sec, 100% production test	V_{ISO}	5000	5000	V_{rms}

1) This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

6.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI1042-DSWVR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{θJA}$ = 100 °C/W[1)], T_J = 150 °C, T_A = 25 °C	1250	mW
Safety Supply Current	$R_{θJA}$ = 100 °C/W[1)], V_I = 5V, T_J = 150 °C, T_A = 25 °C	250	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{θJA}$, of SOP8(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

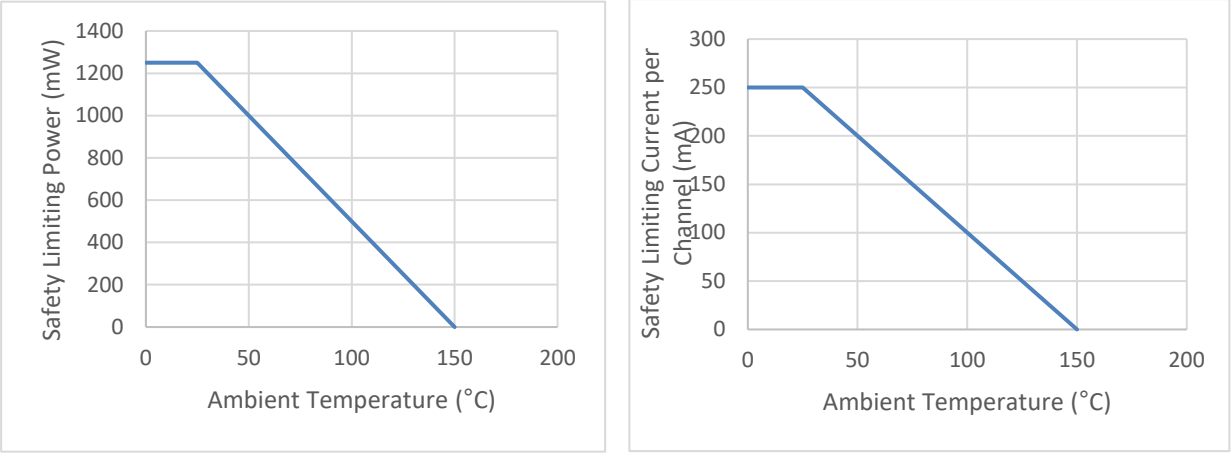


Figure 6.1 NSI1042-DSWVR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI1042-DSWR/NSI1052-DSWR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{θJA}$ = 69.9 °C/W[1)], T_J = 150 °C, T_A = 25 °C	1788	mW
Safety Supply Current	$R_{θJA}$ = 69.9 °C/W[1)], V_I = 5V, T_J = 150 °C, T_A = 25 °C	357	mA

Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

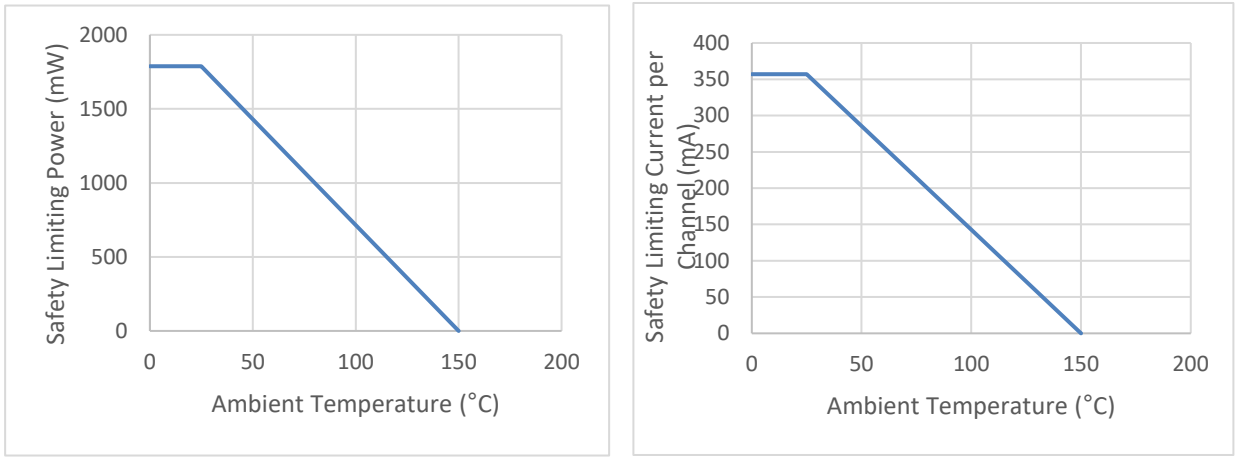


Figure 6.2 NSI1042-DSWR/NSI1052-DSWR Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

6.3. Regulatory information

The NSI1042-DSWR/NSI1052-DSWR is approved by the organizations listed in table.

CUL		***VDE***	***CQC***
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation 2121Vpeak, V_{IOSM}=6250peak	Reinforced insulation
File (E500602)	File (E500602)	File (40052820)	File (CQC20001264939)

The NSI1042-DSWVR is approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation 2121Vpeak, V_{IOSM}=6250peak	Reinforced insulation
File (E500602)	File (E500602)	File (40052820)	File (CQC20001264938)

7. Function Description

The NSI1042 is an isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSI1042 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSI1042 device is safety certified by UL1577 support 5kV$_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSI1042 is up to 5Mbps. The NSI1042 provides thermal protection and transmit data dominant time out function.

7.1. Device Functional Modes

Table 7.1. Driver Function Table

TXD	*CANH*	*CANL*	*BUS STATE*
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

[1] H= high level; L=low level; Z= common mode(recessive) bias to V_{CC}/2

Table 7.2. Receiver Function Table

V_{ID}=CANH-CANL	*RXD*	*BUS STATE*
V_{ID}≥0.9V	L	Dominant
0.5< V_{ID} <0.9V	X	Uncertain
V_{ID}≤0.5V	H	Recessive
Open	H	Recessive

[1] H= high level; L=low level; X= uncertain

7.2. Standby mode

The NSI1052 cannot transmit or receive regular CAN messages in Standby mode. Only the isolator and low-power CAN receiver are active, monitoring the bus lines for activity. The bus wake-up filter ensures that only bus dominant and bus recessive states that persist longer than $t_{filtr(wake)bus}$ are reflected on the RXD pin. To reduce current consumption, the CAN bus is terminated to GND and not biased to VDD2/2 as in Normal mode. Standby mode is selected by setting pin STB HIGH. An internal pull-up ensures that Standby mode is selected by default when pin STB is not connected.

In Standby mode:

• The CAN transmitter if off

• The normal CAN receiver is off

• The low-power CAN receiver is active

• CANH and CANL are biased to GND

• The signal received at the low-power CAN receiver is reflected on pin RXD

The isolation function of the NSI1052 is not disabled in Standby mode. Overall quiescent current is not reduced significantly in this mode. The NSI1052 is not designed to support CAN bus wake-up functionality with very low quiescent currents.

7.3. TXD dominant time-out function

A ‘TXD dominant time-out’ timer circuit prevents the bus lines from being driven to a permanent dominant state(blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

7.4. Bus dominant time-out function

In Standby mode, a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than $t_{to(dom)bus}$, the RXD pin is forced HIGH. This prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

7.5. Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

7.6. Over Temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{TS}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{TS} and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

8. Application Note

8.1. Typical Application

The NSI1042 requires a 0.1 μF bypass capacitors between VDD1 and GND1, VDD2and GND2. The capacitor should be placed as close as possible to the package. The figure8.1 is the basic schematic of NSI1042.

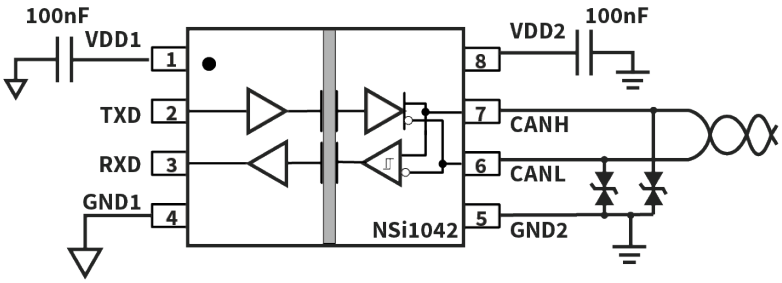


Figure 8.1 Basic schematic of NSI1042

8.2. PCB Layout

The recommended PCB layout shown below.

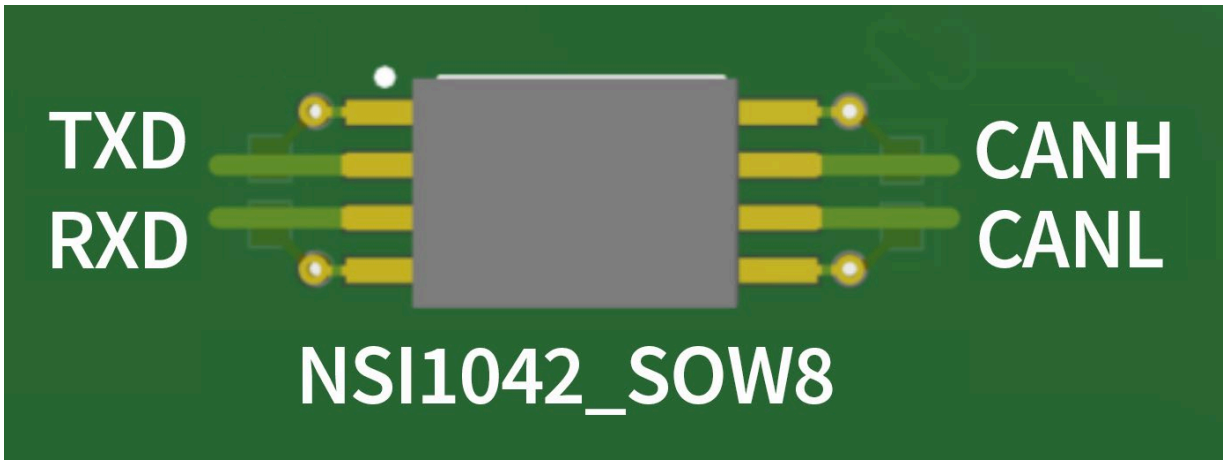


Figure 8.2 Recommended PCB Layout — Top Layer

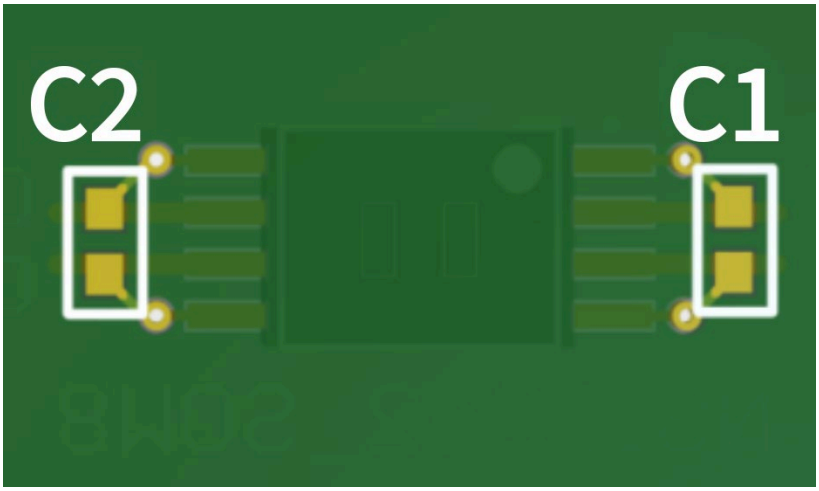
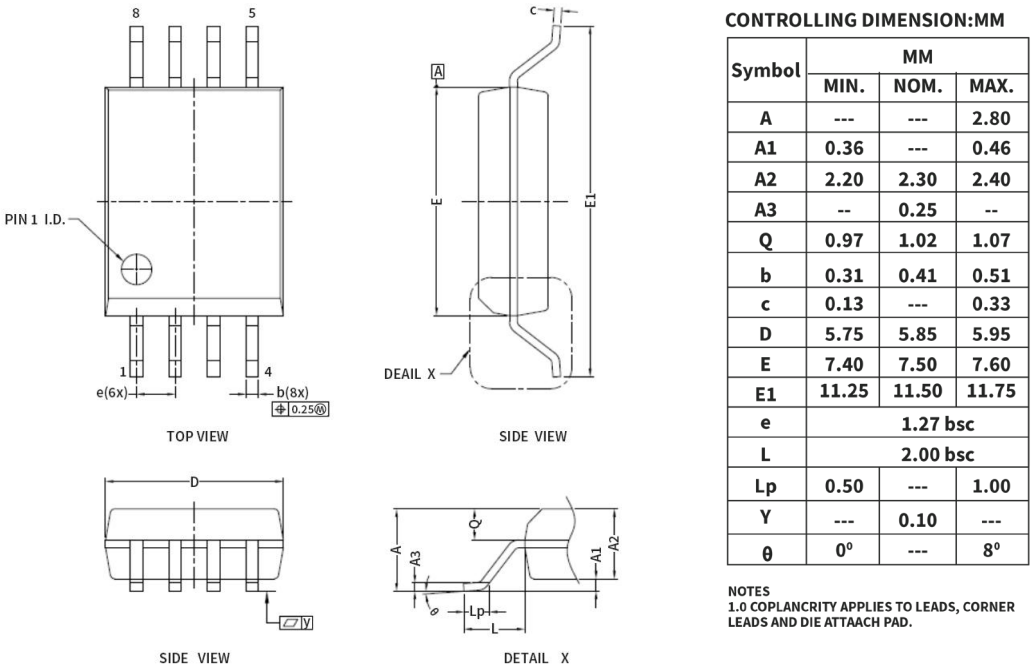


Figure 8.3 Recommended PCB Layout — Bottom Layer

9. Package Information



CONTROLLING DIMENSION:MM

Symbol	MM		
	MIN.	NOM.	MAX.
A	---	---	2.80
A1	0.36	---	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	---	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	---	1.00
Y	---	0.10	---
θ	0°	---	8°

NOTES
1.0 COPLANCRITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTAACH PAD.

Figure 9.1 SOW8 Package Shape and Dimension in millimeters

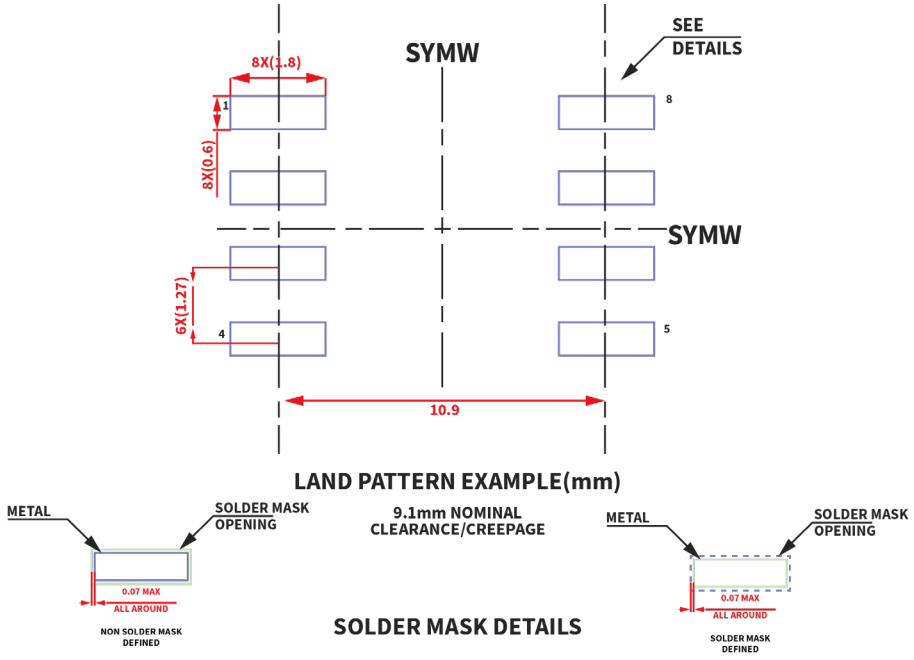
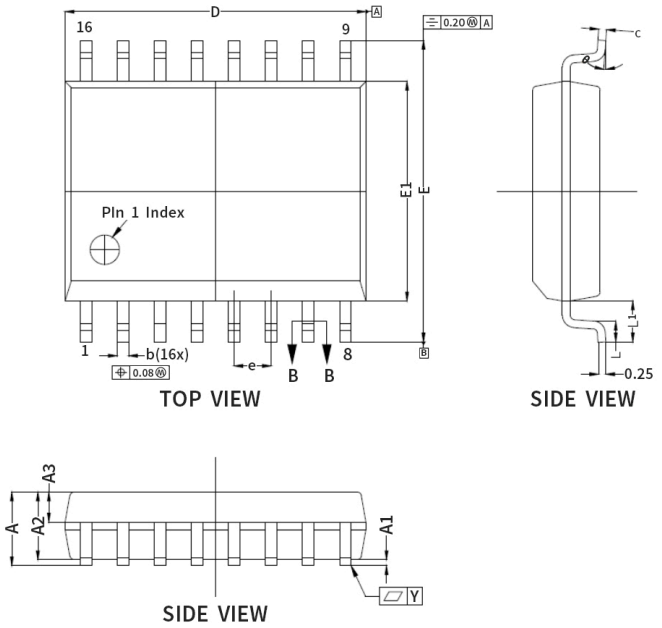


Figure 9.2 SOW8 Package Board Layout Example



CONTROLLING DIMENSION:MM

Symbol	MM		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.11	---	0.30
A2	2.25	2.30	2.35
A3	--	0.25	--
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	2.00 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 9.3 SOW16 Package Shape and Dimension in millimeters

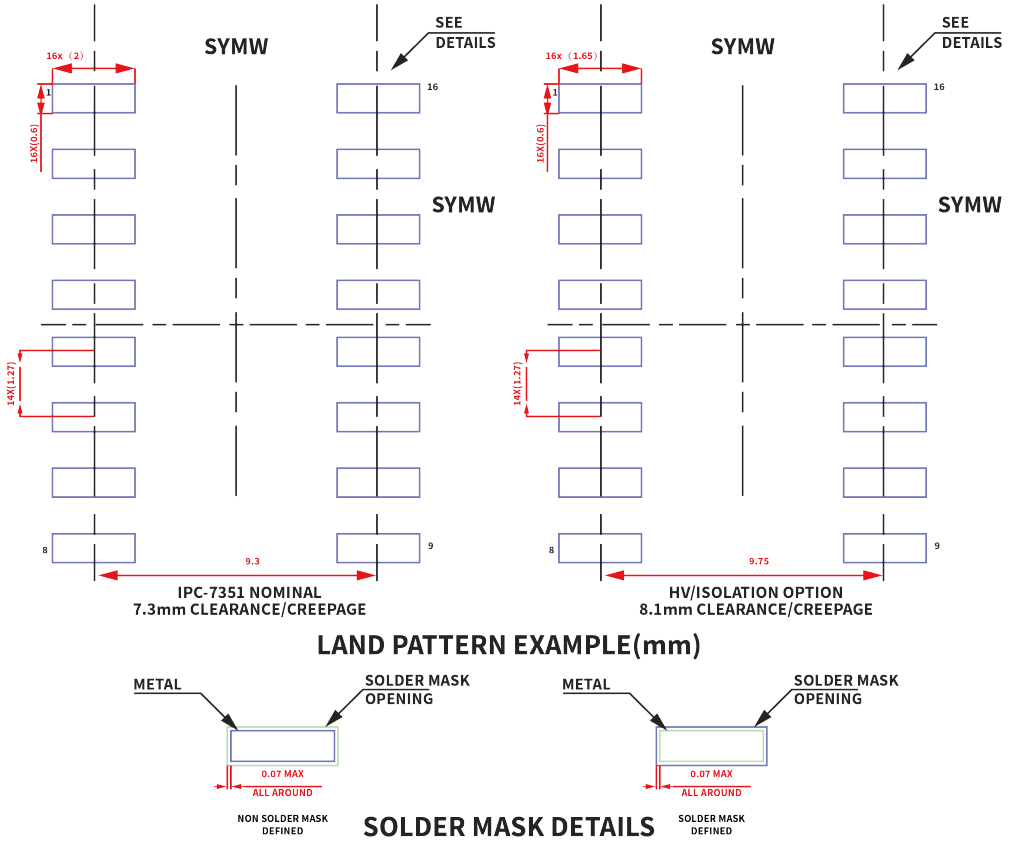


Figure 9.4 SOW16 Package Board Layout Example

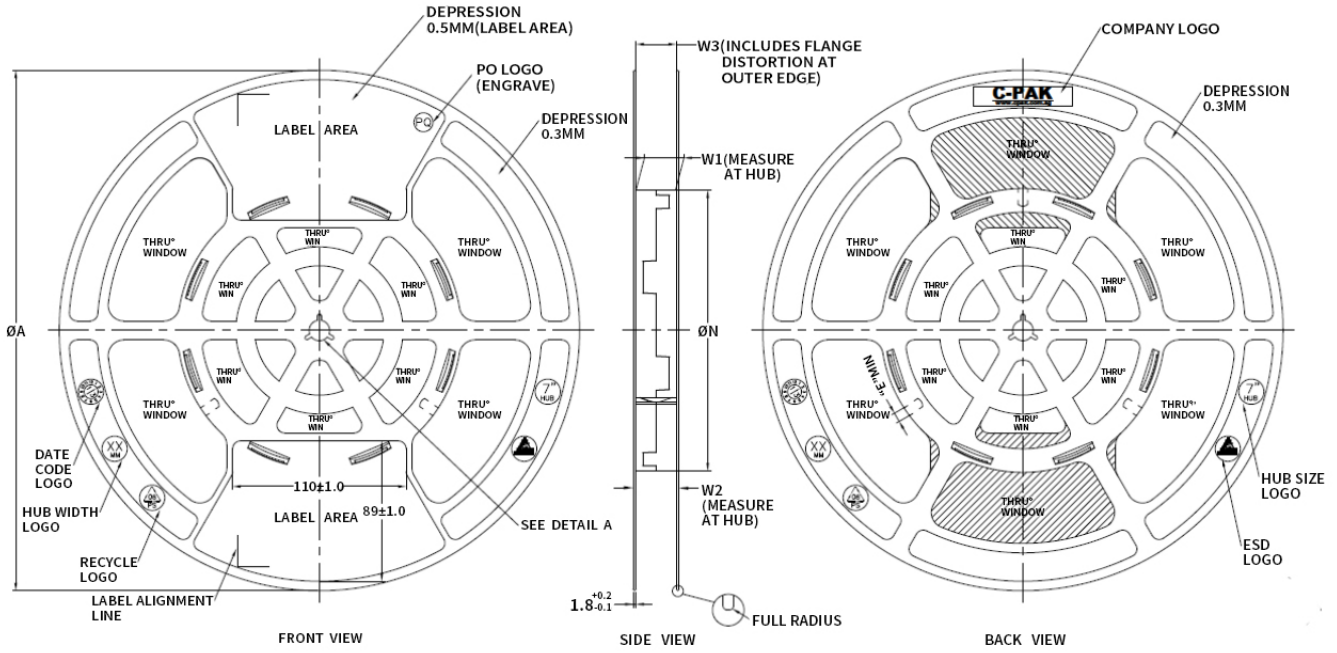
10. Order Information

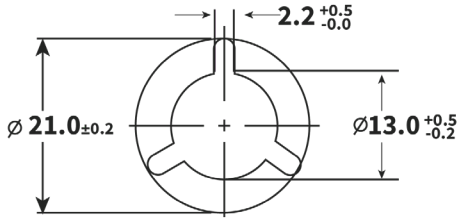
Part Number	*Isolation Rating (kV)*	*Max Data Rate (Mbps)*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NSI1042-DSWVR	5	5 (CAN FD)	-40 to 125℃	3	SOP8 (300mil)	SOW8	1000
NSI1042-DSWR	5	5 (CAN FD)	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NSI1052-DSWR	5	5 (CAN FD)	-40 to 125℃	2	SOP16 (300mil)	SOW16	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.							

11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI1042	Click here	Click here	Click here	Click here

12. Tape and Reel Information





ARBOR HOLE
DETAIL A
SCALE: 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Reel Information (for all packages)

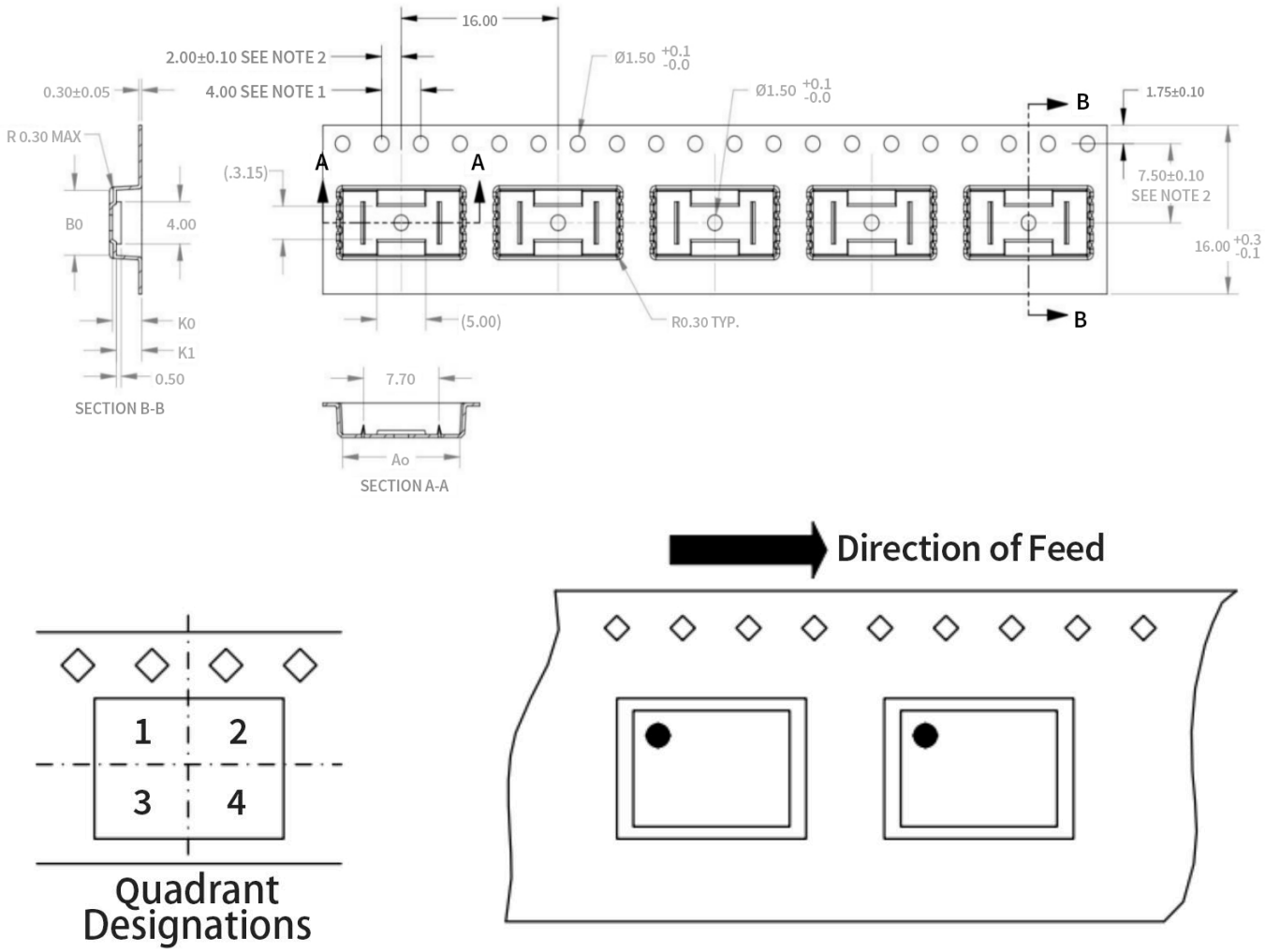
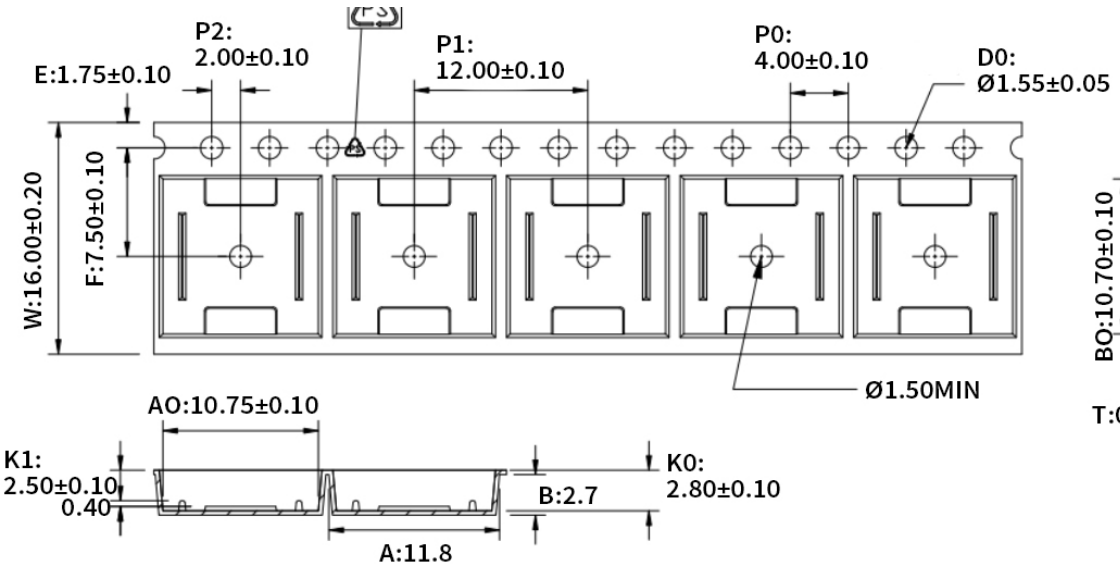


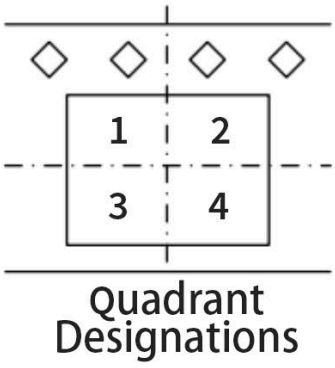
Figure 12.2 Tape Information of SOW8



1.10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30±0.05mm.
6. Packing length per 22" reel: 378 Meters.(復卷 N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:10^{5}~ 10^{10}Ω/口

RoHS

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10



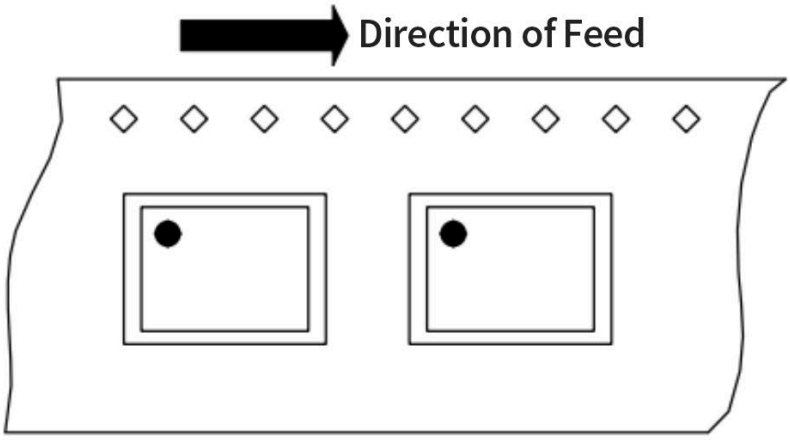


Figure 12.3 Tape and Reel Information of SOW16

13. Revision History

Revision	Description	Date
1.0	Initial version	2021/12/23
1.1	Update thermal temperature, Tape and Reel Information, Package Information	2022/6/14
1.2	Correct figure errors, DTI	2023/2/7
1.3	Update Pin Configuration, Common-mode voltage range, Regulatory Information and Safety Regulatory Approvals. Correct the value of R_{ID} and R_{IN}.	2023/10/30

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