NSD2621X

Half-bridge GaN Driver

Datasheet (EN) 1.2

Product Overview

NSD2621X is an integrated half-bridge gate driver which is designed for GaN HEMT.

The driver operates with a wide supply voltage from 10V to 18V, while internal regulator could offer stable driver voltage to keep GaN FET safe.

The undervoltage lock-out (UVLO) protection feature is provided in low side and high side drivers to prevent the GaN FET from operating in low efficiency or dangerous conditions

The programmable dead-time control function has been provided. The adjustable dead-time range is from 20ns to 100ns.

The device operates in the industrial temperature range, -40°C to 125°C, and is available in a compact 4.0 x 4.0 mm QFN package.

Key Features

- 700V Half-bridge Gate Drivers
- Integrated High-side and Low-side Output Regulators
- UVLO protection on low side and high side
- Source/Sink Current: 2A/ 4A
- Propagation Delay: 30ns TYP
- Short switching delay and mismatch
- Independent turn-on and turn-off adjustable
- Programmable Deadtime from 20ns to 100ns
- Allowable SW slew rate: 150V/ns
- Operating Temperature: -40~125°C
- RoHS & REACH Compliance
- Lead-free component, suitable for lead-free soldering profile: 260°C

Applications

- Driving GaN power FET used in Half-bridge, full-bridge, active flyback or forward, LLC DC-DC converter
- PFC and AC-DC converter
- Industrial Inverters and Motor Drives

Device Information

Part Number	Output	Body Size
NSD2621A-DQAGR	6V	4.0mm x 4.0mm x 0.55mm
NSD2621C-DQAGR	5V	4.0mm x 4.0mm x 0.55mm

Functional Block Diagram

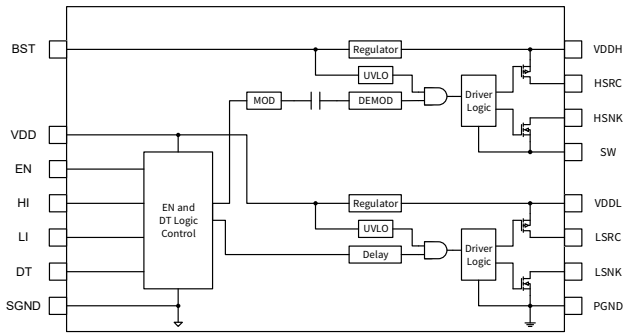


Figure 0.1 NSD2621X Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS 3
2. ABSOLUTE MAXIMUM RATINGS 4
3. ESD RATINGS 4
4. RECOMMENDED OPERATING CONDITIONS 4
5. THERMAL INFORMATION 4
6. SPECIFICATIONS 5
6.1. Electric Characteristics 5
6.2. Dynamic Characteristics 6
6.3. Typical Performance Characteristics 7
6.4. Parameter Measurement Information 10
7. FUNCTION DESCRIPTION 10
7.1. Overview 10
7.2. Under Voltage Lock Out (UVLO) 10
7.3. Regulator Output (VDDL/VDDH) 11
7.4. Input and Output Logic 11
7.5. Programmable Deadtime (DT pin) 12
8. APPLICATION NOTE 13
8.1. Typical Application Circuit 13
8.2. Layout Recommendations 15
9. PACKAGE INFORMATION 17
10. ORDERING INFORMATION 18
11. TAPE AND REEL INFORMATION 18
12. REVISION HISTORY 20

1. Pin Configuration and Functions

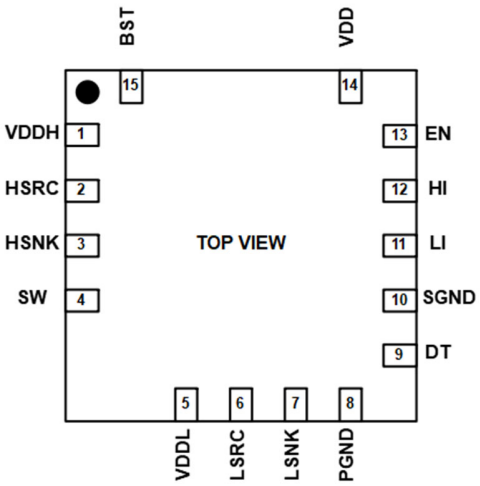


Figure 1.1 Pin Configuration

Table 1.1 Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	VDDH	High-side voltage regulator output. A ceramic capacitor of not less than 100nF must be connected between VDDH and SW.
2	HSRC	High-side driver sourcing output
3	HSNK	High-side driver sinking output
4	SW	High-side driver reference (Switching node)
5	VDDL	Low-side voltage regulator output. A ceramic capacitor of not less than 100nF must be connected between VDDL and PGND.
6	LSRC	Low-side driver sourcing output
7	LSNK	Low-side driver sinking output
8	PGND	Low-side driver reference (Power ground)
9	DT	Dead-time adjustment
10	SGND	Signal ground
11	LI	Low-side driver logic input
12	HI	High-side driver logic input
13	EN	Dual drivers enabling logic input
14	VDD	Power supply for logic and low-side regulator
15	BST	Power supply for high-side regulator (Bootstrap voltage)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
High-side Common Mode Voltage	V_{SW}	-700	720	V
Driver Supply Voltage	VDD to SGND, BST to SW	-0.3	24	V
Regulator Output Voltage	VDDL to PGND, VDDH to SW	-0.3	7	V
Different Ground Voltage	SGND to PGND	-5	5	V
Input Signal Voltage	HI, LI, EN, DT to SGND	-0.3	V_{VDD}+0.3	V
	HI, LI, EN, DT to SGND, Transient for 50ns	-5	V_{VDD}+0.3	V
Driver Output Voltage	LSRC/LSNK to PGND, HSRC/HSNK to SW	-0.3	V_{VDDL}+0.3, V_{VDDH}+0.3	V
	LSRC/LSNK to PGND, HSRC/HSNK to SW, Transient for 50ns	-2	7	V
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-55	150	°C

3. ESD RATINGS

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD	±3000	V
	Charged device model (CDM), per AEC-Q100-011-RevB	±1000	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
High-side Common Mode Voltage	V_{SW}	0	650	V
Driver Supply Voltage	VDD to SGND, BST to SW	10	18	V
Driver Output Voltage	LSRC/LSNK to PGND, HSRC/HSNK to SW	0	V_{VDDL}, V_{VDDH}	V
Input Signal Voltage	HI, LI, EN to SGND	0	V_{VDD}	V
Ambient Temperature	T_a	-40	125	°C

5. Thermal Information

Parameters	Symbol	Value	Unit
Junction-to-ambient thermal resistance[1)]	θ_{JA}	81	°C/W
Junction-to-case(top) thermal resistance[1)]	$\theta_{JC(top)}$	24	°C/W

Parameters	Symbol	Value	Unit
Junction-to-board thermal resistance[1)]	θ_{JB}	71	°C/W
Junction-to-top characterization parameter[1)]	Ψ_{JT}	61	°C/W
Junction-to-board characterization parameter[1)]	Ψ_{JB}	55	°C/W

1) High Effective Thermal Conductivity Test Board (2s2p) in an environment described in JESD51-2a.

6. Specifications

6.1. Electric Characteristics

VDD = 12V, T_a = -40°C to 125°C. Unless otherwise noted, Typical values are at T_a= 25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Driver Power Supply						
VDD Quiescent Current	I_{VDDQ}		0.42		mA	HI = LI = 0V
VDD Operating Current	I_{VDDO}		2.6		mA	HV = SW = 0V, BST = 12V, f = 500kHz， C_{load} = 330pF
BST Quiescent Current	I_{BSTQ}		0.58		mA	HI = LI = 0V
BST Operating Current	I_{BSTO}		2.7		mA	HV =SW = 0V, BST = 12V, f = 500kHz， C_{load} = 330pF
VDD UVLO Rising Threshold	V_{VDD_ON}	8.0	8.4	8.8	V	
VDD UVLO Falling Threshold	V_{VDD_OFF}	7.5	7.8	8.1	V	
VDD UVLO Hysteresis	V_{VDD_HYS}	0.4	0.6		V	
BST UVLO Rising Threshold	V_{BST_ON}-V_{SW}	8.0	8.4	8.8	V	
BST UVLO Falling Threshold	V_{BST_OFF}-V_{SW}	7.5	7.8	8.1	V	
BST UVLO Hysteresis	V_{BST_HYS}	0.4	0.6		V	
Input Logic						
Input Pin Pull-down Resistance	R_{HI_PD}, R_{LI_PD}		200		kΩ	HI = LI = 3V
Enable Pin Pull-down Resistance	R_{EN_PD}		200		kΩ	EN = 3V
Input Pin High Logic Bias Current	I_{HI_H}, I_{LI_H}		20		μA	HI = LI = 5V
Enable Pin High Logic Bias Current	I_{EN_H}		20		μA	EN = 5V
Logic High Input Threshold	V_{HI_H}, V_{LI_H}	1.7	2.1	2.5	V	
Logic Low Input Threshold	V_{HI_L}, V_{LI_L}	0.9	1.2	1.5	V	
Input Hysteresis	V_{HI_HYS}, V_{LI_HYS}	0.7	0.9		V	
Logic High Input Threshold	V_{EN_H}	1.7	2.1	2.5	V	
Logic Low Input Threshold	V_{EN_L}	0.9	1.4	1.5	V	

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Input Hysteresis	V_{EN_HYS}	0.5	0.7		V	
Driver Output Characteristic						
Regulator Output Voltage	V_{VDDL}, V_{VDDH}-V_{SW}	5.6	6	6.3	V	C_{VDDL} = 100nF, $C_{VDDH-SW}$ = 100nF, NSD2621A
		4.6	5	5.4	V	C_{VDDL} = 100nF, $C_{VDDH-SW}$ = 100nF, NSD2621C
Regulator UVLO Rising Threshold	V_{VDDH_ON}, V_{VDDL_ON}	4.1	4.4	4.7	V	
Regulator UVLO Falling Threshold	V_{VDDH_OFF}, V_{VDDL_OFF}	3.8	4.1	4.4	V	
Regulator UVLO Hysteresis	V_{VDDH_HYS}, V_{VDDL_HYS}		0.3		V	
High−level output voltage, V_{VDDH}−V_{HSRC} or V_{VDDL}−V_{LSRC}	V_{OH}		16		mV	I_xSRC = 10 mA
Low−level output voltage, V_{HSNK}−V_{SW} or V_{LSNK} −PGND	V_{OL}		8		mV	I_xSNK = 10 mA
Output Peak Source Current	I_{LSRC_PK}, I_{HSRC_PK}		2		A	
Output Peak Sink Current	I_{LSNK_PK}, I_{HSNK_PK}		4		A	

6.2. Dynamic Characteristics

VDD=12V, T_a=-40°C to 125°C. Unless otherwise noted, Typical values are at T_a=25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Minimum Input Pulse Width	t_{PWmin}			20	ns	
Output Rising Time	t_{LSRC}/t_{HSRC}		6		ns	C_{load} = 330pF
Output Falling Time	t_{LSNK}/t_{HSNK}		5		ns	C_{load} = 330pF
Turn-on Propagation Delay Time	$t_{PD(on)}$		30	60	ns	
Turn-off Propagation Delay Time	$t_{PD(off)}$		30	60	ns	
Propagation Delay Match	t_{PDM}			10	ns	
Pulse Width Distortion	t_{PWD}			10	ns	
VDD or BST Power-up Delay Time[1)]	t_{PUD}		15		µs	First time power-up from V_{POR}
VDDL or VDDH Rising Time[1)]	t_{VDDL_R}/ t_{VDDH_R}		13		µs	C_{VDDL}= 100nF, $C_{VDDH-SW}$ = 100nF
Programmed Deadtime	t_{DT_Min}		20		ns	R_{DT} <= 20kΩ or R_{DT}>620kΩ, C_{DT} = 1nF
	t_{DT_Linear}		R_{DT}(kΩ)		ns	35kΩ< R_{DT} <= 100kΩ, C_{DT} = 1nF
	t_{DT_Max}		100		ns	110kΩ<R_{DT} <= 220kΩ, C_{DT} = 1nF

1) See detail in Figure 7.1.

6.3. Typical Performance Characteristics

T_a= 25°C, unless otherwise noted.

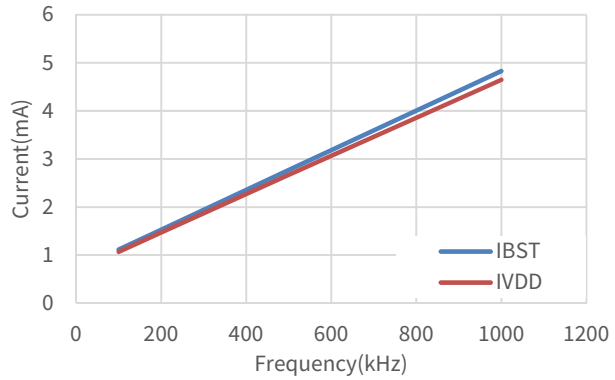


Figure 6.1 Operating Current (I_VDD, I_BST) vs. Frequency (VDD = VBST=12 V, SW = PGND, 330pF load)

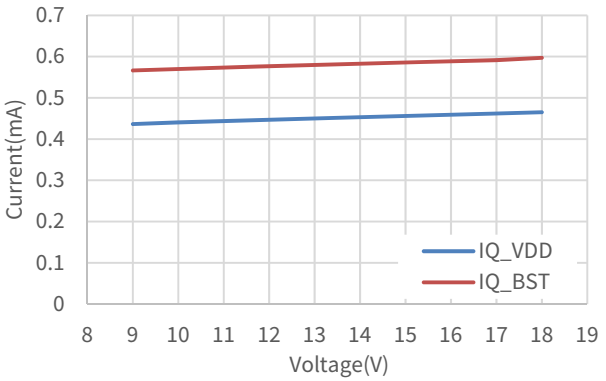


Figure 6.2 Quiescent Current (IQ_VDD, IQ_BST) vs. Voltage

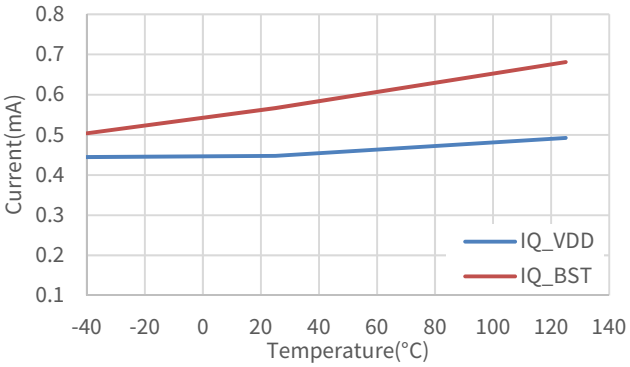


Figure 6.3 Quiescent Current (IQ_VDD, IQ_BST) vs. Temperature

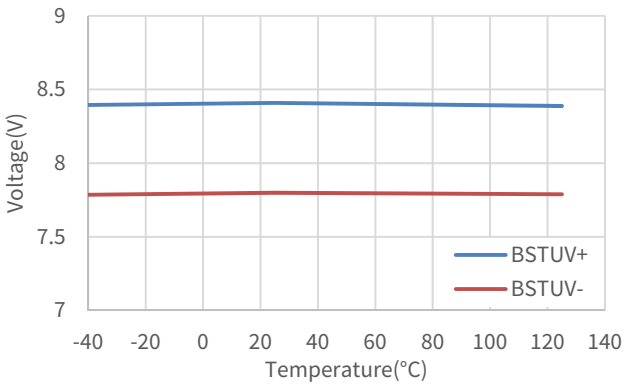


Figure 6.4 BST UVLO vs. Temperature

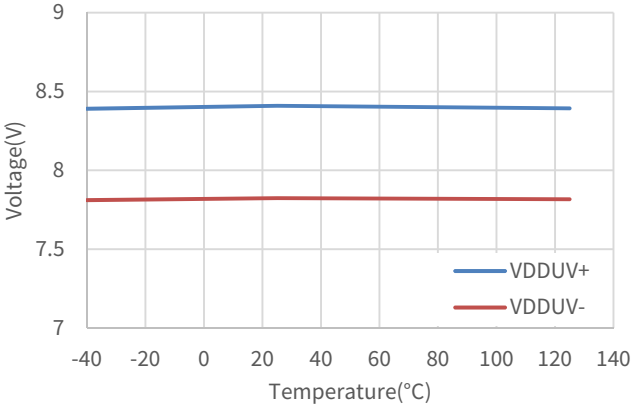


Figure 6.5 VDD UVLO vs. Temperature

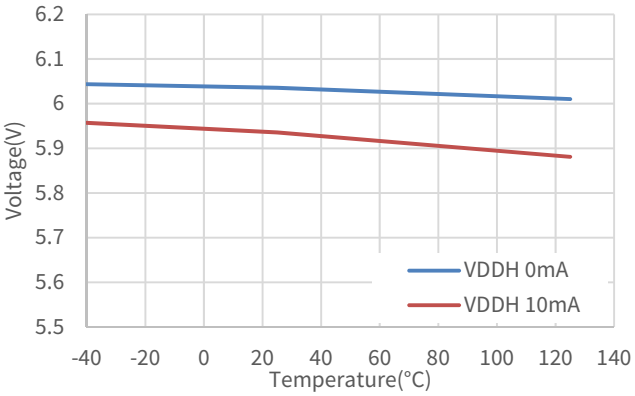


Figure 6.6 VDDH Output Voltage vs. Temperature

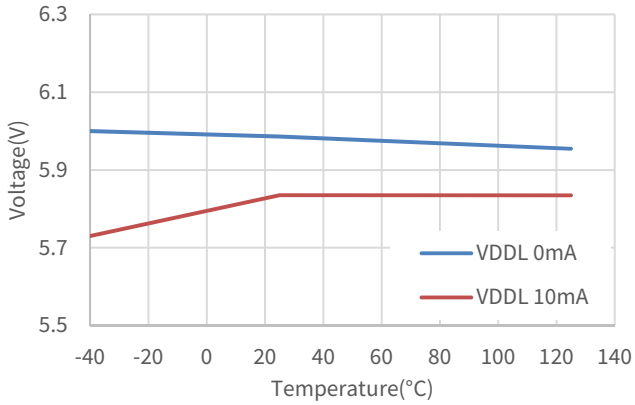


Figure 6.7 VDDL Output Voltage vs. Temperature

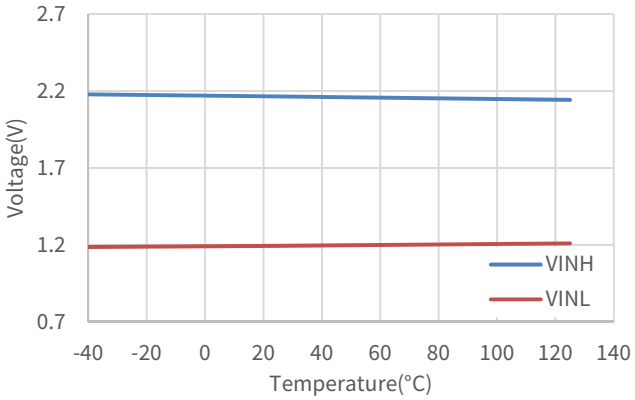


Figure 6.8 Input Logic (HI, LI) Threshold vs. Temperature

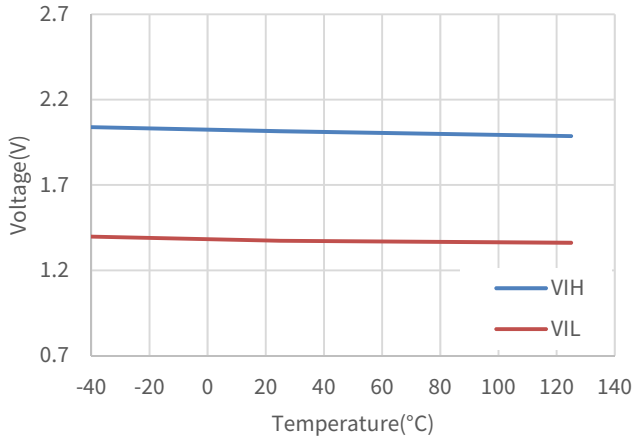


Figure 6.9 Input Logic (EN) Threshold vs. Temperature

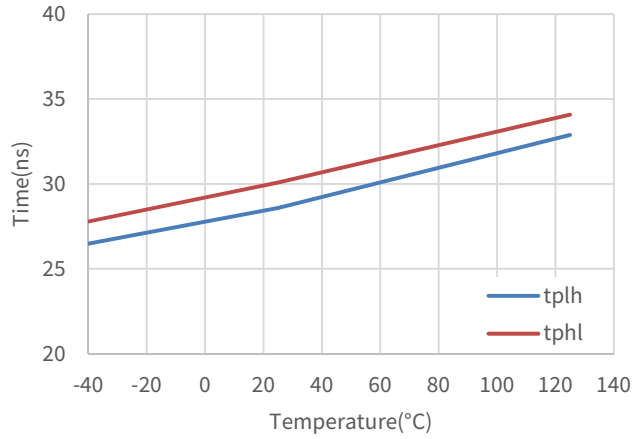


Figure 6.10 LI to LSRC & LSNK Propagation Delay vs. Temperature

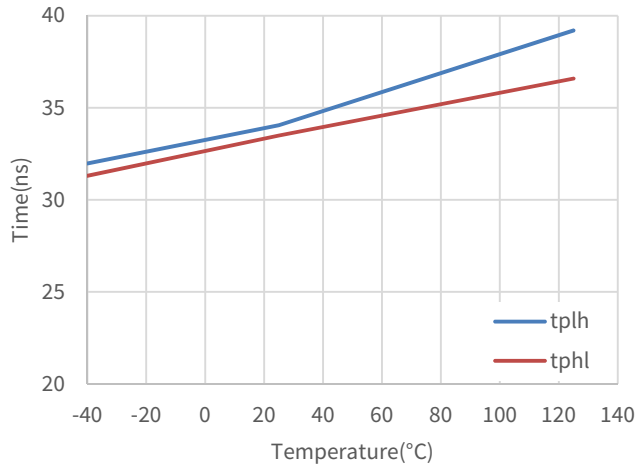


Figure 6.11 HI to HSRC & HSNK Propagation Delay vs. Temperature

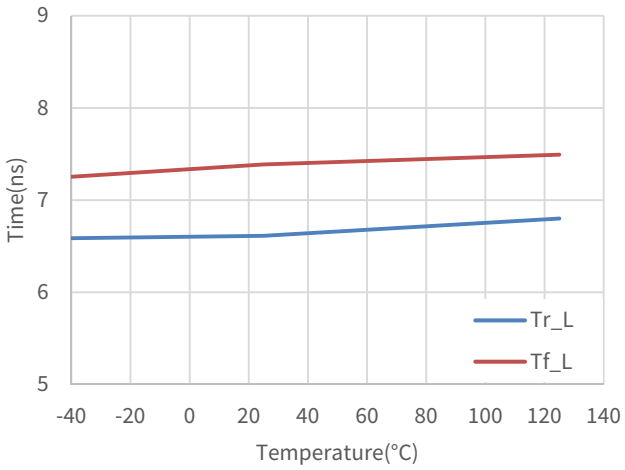


Figure 6.12 LSRC Rise Time and LSNK Fall Time vs. Temperature

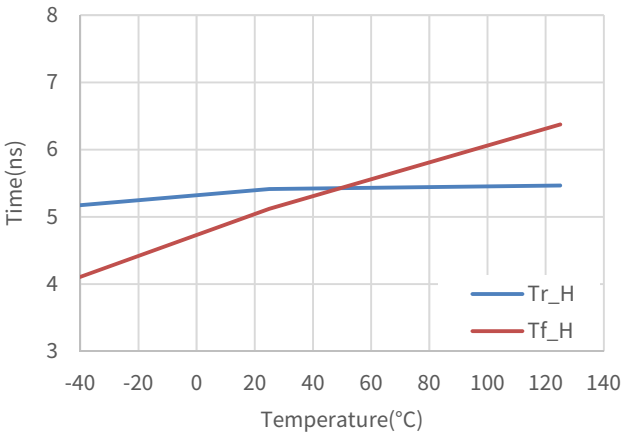


Figure 6.13 HSRC Rise Time & HSNK Fall Time vs. Temperature

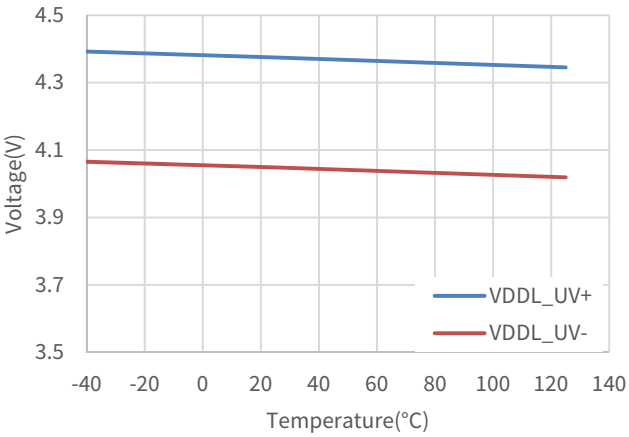


Figure 6.14 VDDL UVLO vs. Temperature

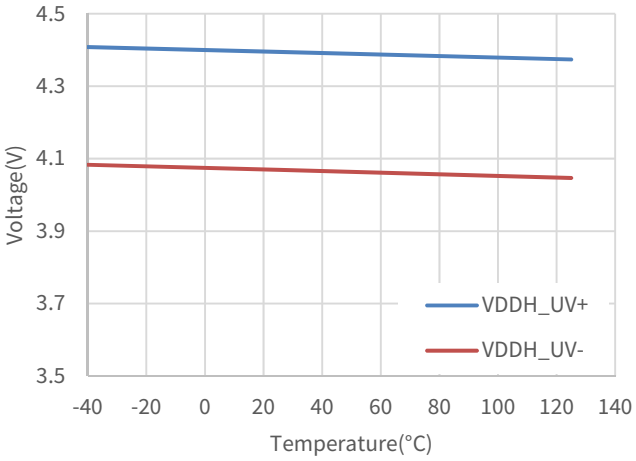


Figure 6.15 VDDH UVLO vs. Temperature

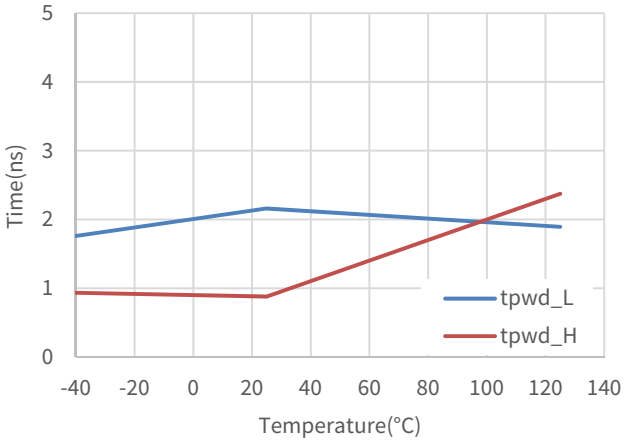


Figure 6.16 Pulse Width Distortion vs. Temperature

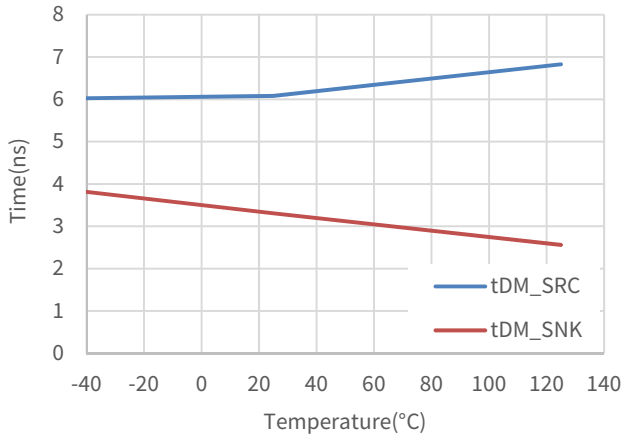


Figure 6.17 Propagation Delay Matching (HI to HO, LI to LO) vs. Temperature

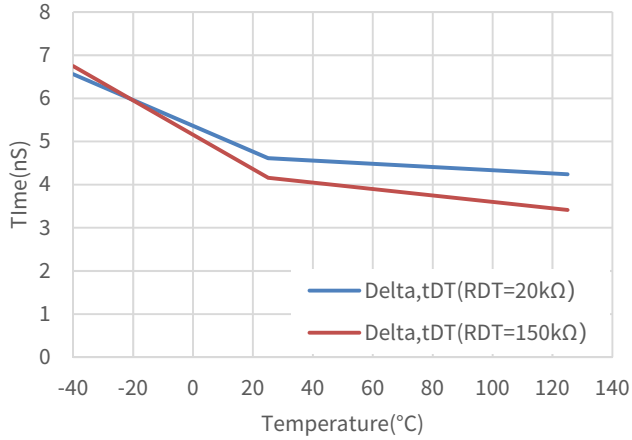


Figure 6.18 Dead−time Mismatch vs. Temperature

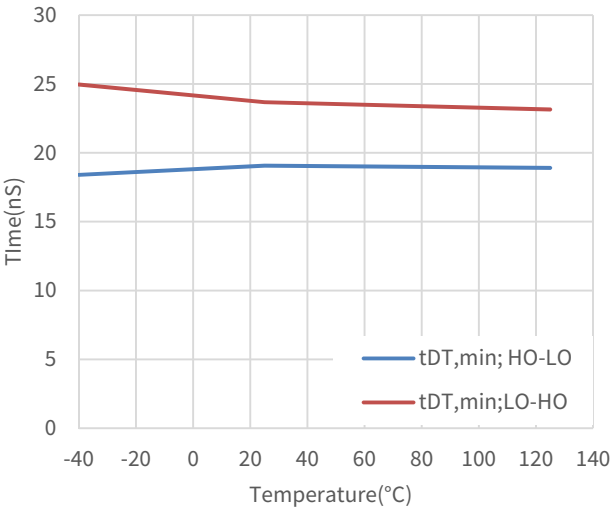


Figure 6.19 Minimum Dead−time (RDT = 20kΩ) vs. Temperature

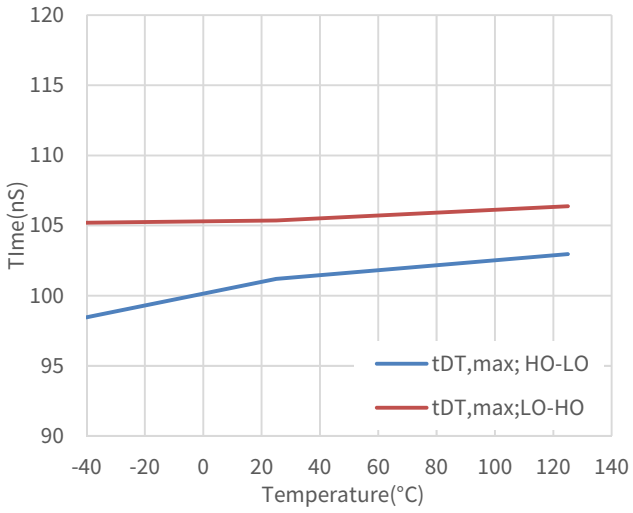


Figure 6.20 Maximum Dead−time (RDT = 150kΩ) vs. Temperature

6.4. Parameter Measurement Information

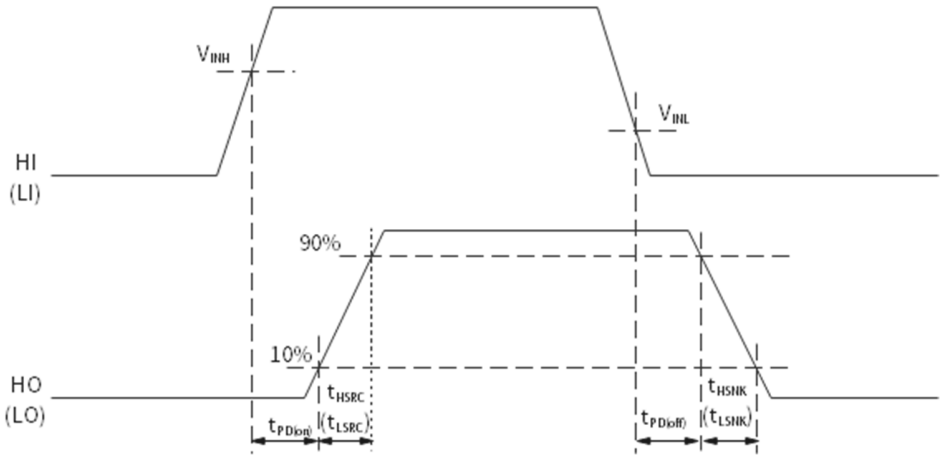


Figure 6.21 Switching Time Waveform

7. Function Description

7.1. Overview

NSD2621X is an integrated half-bridge gate driver for GaN FET. In order to output stable driver voltage, it integrated the regulator and draws out the output of regulator. The source and sink of gate driver were separated, which is convenient for users to adjust he switching speed of GaN FET. In addition, it also provides the programmable deadtime and under voltage lock out (UVLO) protection.

7.2. Under Voltage Lock Out (UVLO)

The NSD2621X has internal under voltage lock out (UVLO) protections on low side and high side power supply blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDD or BST is lower than V_{VDD_ON} / V_{BST_ON} at power-up status

or lower than V_{VDD_OFF} / V_{BST_OFF} after power-up, regardless of the status of the input pins.

The 0.6V hysteresis (V_{VDD_HYS}) on VDD and BST ULVO protections are provided prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup. When VDD voltage or BST voltage is more than V_{VDD_POR} / V_{BST_POR} which is approximate 2V, the internal part circuits will begin to operate. In Figure.6.1, t_{PUD} is the power up delay time which is about 22us.

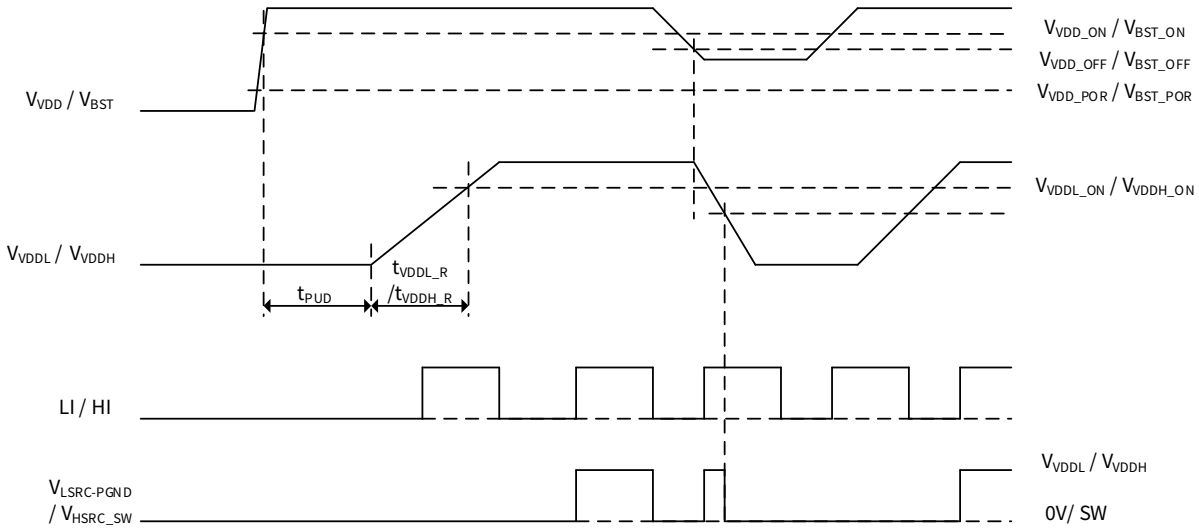


Figure 7.1 UVLO Diagram

7.3. Regulator Output (VDDL/VDDH)

The NSD2621X integrated the linear regulator in the low side and high side and VDDL/VDDH is the output of regulator. The VDDL regulator is fed directly from VDD and directedly provide the driver voltage and current for low side GaN FET. The VDDL regulator is referenced to the power ground (PGND) pin. Source current for the low−side GaN FET is provided from the charge stored in the capacitor connected between VDDL and PGND. A not less than 100nF ceramic capacitor must be used on VDDL to normally operate. When the VDDL voltage is higher than 4.4V which is UVLO rising threshold (V_{VDDL_ON}), the output enables; When the VDDL voltage is lower than 4.1V which is UVLO falling threshold (V_{VDDL_OFF}), the output disables.

The VDDH regulator is fed directly from BST and directedly provide the driver voltage and current for high side GaN FET. The VDDH regulator is referenced to SW. Source current for the how−side GaN FET is provided from the charge stored in the capacitor connected between VDDH and SW. A not less than 100nF ceramic capacitor must be connected between VDDH and SW pins. When the VDDH voltage is higher than 4.4V which is UVLO rising threshold (V_{VDDH_ON}), the output enables; When the VDDH voltage is lower than 4.1V which is UVLO falling threshold (V_{VDDH_OFF}), the output disables.

7.4. Input and Output Logic

The NSD2621X is a half-bridge gate driver with dead-time control. The EN pin should be logic high to keep the driver operating normally.

Table 7.1 Output status vs. Input and Power status

Input Pins			Output Pins		NOTE
EN	HI	LI	HSRC/HSNK	LSRC/LSNK	
L or O	X	X	L	L	
H	L	L	L	L	

Input Pins			Output Pins		NOTE
EN	HI	LI	HSRC/HSNK	LSRC/LSNK	
H	L	H	L	H	Driver's outputs turn on after the deadtime expires.
H	H	L	H	L	
H	H	H	L	L	The input signal is later than VDD power up.

1) H= Logic High; L= Logic Low; O= Left Open; X= Irrelevant.

7.5. Programmable Deadtime (DT pin)

The NSD2621X has a programmable deadtime control function by placing a resistor, R_{DT}, between the DT pin and SGND. The relationship between deadtime and R_{DT} has been shown in Figure 7.2.

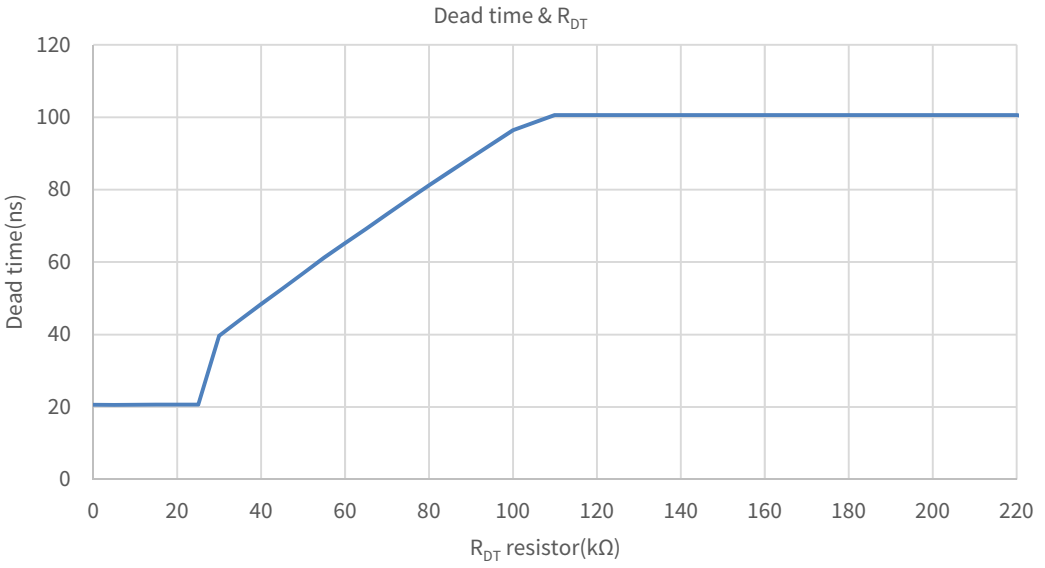


Figure 7.2 Dead time

1) While R_{DT} is lower than 20kΩ or higher than 620kΩ, the deadtime duration (t_{DT}) is set to 20ns.
2) While R_{DT} is in the range of 35kΩ to 100kΩ, the t_{DT} can be determined from Equation 1, where R_{DT} is in kΩ and t_{DT} in ns:

$$t_{DT} \approx 1 \times R_{DT} \quad (1)$$

3) While R_{DT} is in range of 110kΩ to 220kΩ, the deadtime duration (t_{DT}) is set to 100ns.

The recommended value of R_{DT} is from 1kΩ to 200kΩ. The accuracy of dead time is ±25%. It is also recommended to parallel a ceramic capacitor, for example 1nF, with R_{DT} to achieve better noise immunity.

The programmed deadtime is activated by the input signal's falling edge to prevent shoot-through when the device is designed in an application of high side and low side driver. The details of input and output logic with deadtime are shown as Figure 7.3:

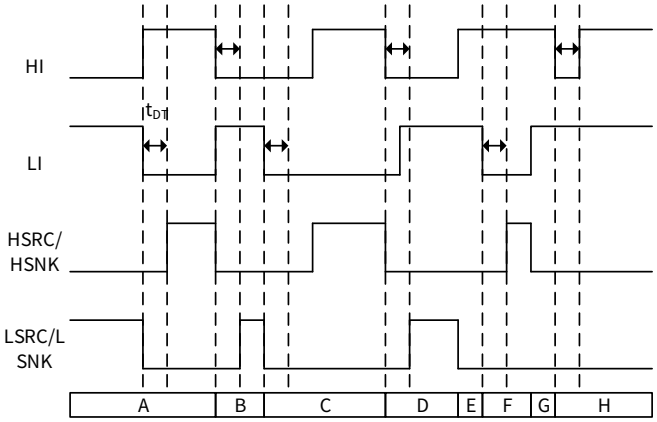


Figure 7.3 Input and Gate Logic with the Programmed Deadtime

Condition	*Result*
A: HI goes high, and LI goes low.	LSRC/LSNK goes low immediately, then HSRC/HSNK goes high after the programmed deadtime which is assigned at LI goes low.
B: HI goes low, and LI goes high.	HSRC/HSNK goes low immediately, then LSRC/LSNK goes high after the programmed deadtime which is assigned at HI goes low.
C: LI goes low, then HI goes high after deadtime.	LSRC/LSNK goes low immediately, then HSRC/HSNK goes high immediately when HI goes high.
D: HI goes low, then LI goes high before deadtime.	HSRC/HSNK goes low immediately, then LSRC/LSNK goes high after deadtime
E: HI goes high, LI is still high.	LSRC/LSNK goes low immediately, and HSRC/HSNK keeps low.
F: HI is still high, LI goes low.	HSRC/HSNK goes high after deadtime while LI is low, and LSRC/LSNK keeps low.
G: HI is still high, LI goes high after deadtime	HSRC/HSNK goes low immediately, and LSRC/LSNK keeps low.
H: HI goes low then goes high before deadtime while LI is still high.	HSRC/HSNK keeps low and LSRC/LSNK keeps low because deadtime control.

8. Application Note

8.1. Typical Application Circuit

Figure. 8.1 shows a typical half-bridge configuration by using the NSD2621X.

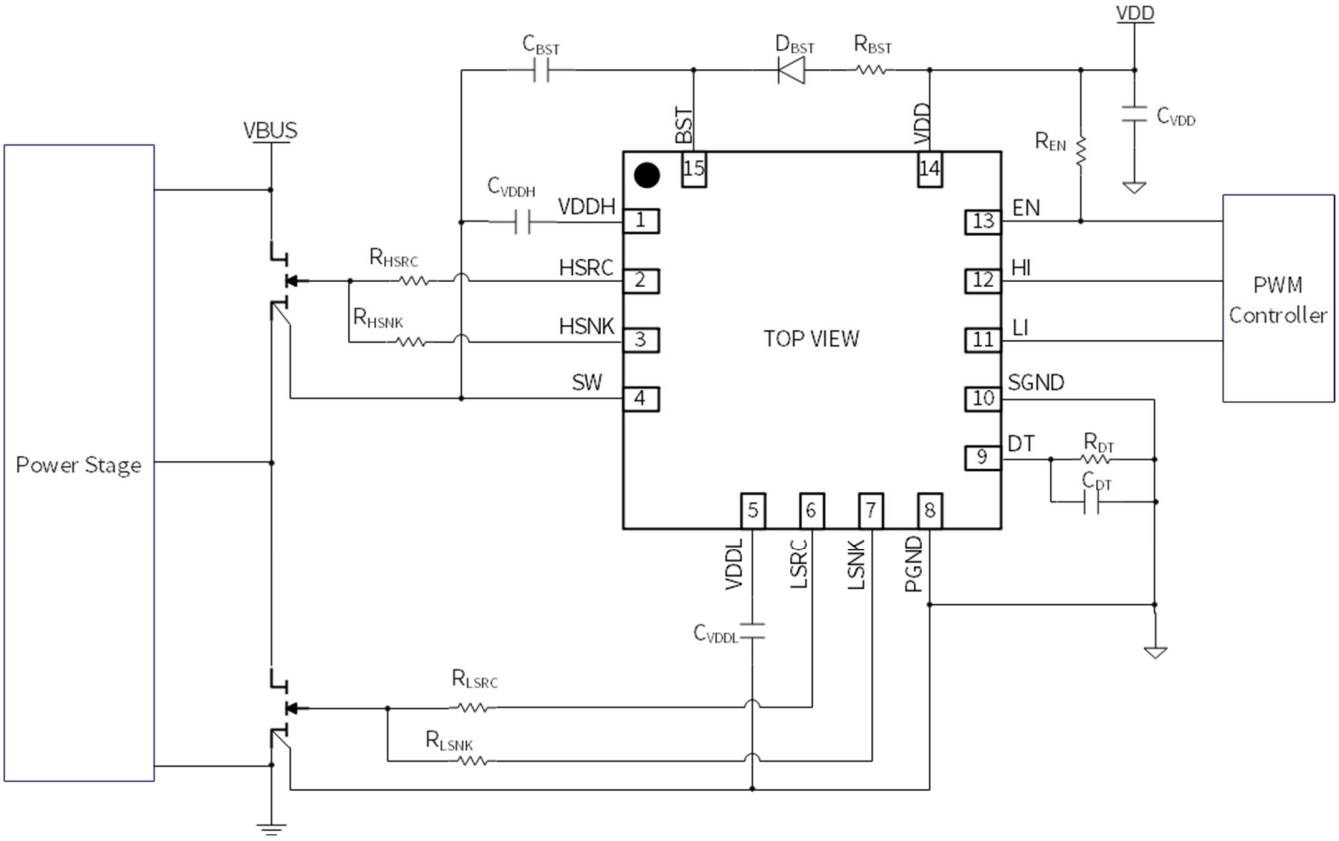


Figure. 8.1 Simplified Half-Bridge Application Schematic

Supply voltage (VDD): VDD is the low side power supply of NSD2621X. It provides the power for digital inputs, internal logic functions and the internal low−side regulator (VDDL). A single VDD bypass capacitor, C_{VDD}, is required and connected directly between the VDD and SGND pins. The C_{VDD} capacitor should be a ceramic bypass capacitor > 100 nF, located as close as possible to the VDD and SGND pins to properly filter out all glitches while switching.

High-Side Bootstrap Voltage (BST): BST is the high side power supply of NSD2621X. The BST voltage is input to an internal regulator which produces the VDDH voltage. The resistor R_{BST} is series connected with D_{BST} to limit the bootstrap current. The bootstrap capacitor C_{BST} connected directly between BST and SW pins. The capacitor C_{BST} should be a ceramic capacitor and located as close as possible to the BST and SW pins to properly filter out all glitches while switching. The value of C_{BST} should be large to provide fully charge for high side normal operation. No high side pulses are produced when the voltage on BST pin is less than UVLO voltage.

The bootstrap diode D_{BST} should be high−speed, low leakage current and very low junction capacitance. Its rated voltage must be greater than VBUS.

The purpose of the bootstrap resistor R_{BST} is to limit peak charging current of C_{BST}, especially during startup. A too small resistor may not limit the peak current enough, resulting in excessive ringing which can cause jitter in the high side gate drive or EMI problems. A large resistor will dissipate more power and create a longer RC time constant causing a longer start up time. A bootstrap resistor in the range of $1\Omega < R_{BST} < 10\Omega$ is usually sufficient.

Low Side Regulator (VDDL): VDDL is the low side regulator output. The VDDL regulator is fed directly from VDD and directedly provide the drive voltage and current for low side GaN FET. The VDDL regulator is referenced to the power ground (PGND) pin. The VDDL output voltage is respectively 6Vand 5V for NSD2621A/ C. Source current for the low−side GaN FET is provided from the charge stored in the capacitor C_{VDDL} connected between VDDL and PGND. A not less than 100nF ceramic capacitor C_{VDDL} must be connected

between VDDL and PGND pins. The VDDL regulator will not output when VDD voltage is less than UVLO voltage. When the VDDL voltage is higher than 4.4V which is UVLO threshold (V_{VDDL_ON}), the output enables; When the VDDL voltage is lower than 4.1V which is UVLO threshold (V_{VDDL_OFF}), the output disables.

High Side Regulator (VDDH): VDDH is the high side regulator output. The VDDH regulator is fed directly from BST and directedly provide the drive voltage and current for high side GaN FET. The VDDH regulator is referenced switching node (SW) pin. The VDDH output voltage is respectively 6V and 5V for NSD2621A/ C. Source current for the high side GaN FET is provided from the charge stored in the capacitor C_{VDDH} connected between VDDH and SW. A not less than 100nF ceramic capacitor C_{VDDH} must be connected between VDDH and SW pins. The VDDH regulator will not output when BST voltage is lower than UVLO voltage. When the VDDH voltage is higher than 4.4V which is UVLO threshold (V_{VDDH_ON}), the output enables; When the VDDH voltage is lower than 4.1V which is UVLO threshold (V_{VDDH_OFF}), the output disables.

Signal Ground (SGND) and Power Ground (PGND): SGND is the PGND for all internal control logic and digital inputs. Internally, the SGND and PGND pins are isolated from each other. PGND is the return reference of the low side gate drive and VDDL. For GaN FETs that include a source Kelvin return, a direct connection should be made from PGND to the GaN FET Kelvin return. C_{VDDL} should be referenced to the PGND but separate from the power stage ground as shown in Figure. 8.1

The NSD2621X low side drive circuit is able to withstand −5 V to +5 V of common mode voltage between SGND and PGND. If the common mode voltage is over the range, NSD2621X may be damaged. In practical application, SGND and PGND should be connected together with a low impedance resistor or with a short low impedance trace on the PCB.

Switch Node (SW): SW is the return reference of high side gate drive. For GaN FETs included a source Kelvin return, a direct connection should be made from SW to the GaN FET Kelvin return. C_{VDDH} and C_{BST} should be referenced to the SW pin but separate from the power stage switch node as shown in Figure. 8.1

Input (LI, HI): LI and HI are the PWM signal input pins. Both inputs are independent and internally pulled low to SGND such that each output is defaulted to be low. The input is compatible with Transistor-Transistor Logic (TTL).

Enable (EN): Enable (EN) is internally pulled low to SGND so that the driver is defaulted to a disabled output status. EN voltage is above 2.5V maximum, enables the outputs. EN can be controlled by digital signal or connected directly VDD. If EN is pulled low during normal operation, the driver outputs are immediately disabled.

Deadtime (DT): A resistor R_{DT} should be connected between DT and SGND pins in order to configure the deadtime. The recommended value of R_{DT} is between from 1kΩ to 200kΩ. It is also recommended to parallel a ceramic capacitor, for example 1nF, with R_{DT} to achieve better noise immunity.

High Side Output (HSRC and HSNK): HSRC and HSNK control turn-on and turn-off of high side GaN FET respectively. This allows a single resistor between each pin and the gate of high side GaN FET to independently control gate rising and falling speed.

Ligh Side Output (LSRC and LSNK): LSRC and LSNK control turn-on and turn-off of low side GaN FET respectively. This allows a single resistor between each pin and the gate of low side GaN FET to independently control gate rising and falling speed.

8.2. Layout Recommendations

PCB layout is important to get optimal performance. Some of the layout guidelines to be followed are listed below:

1) The bypass capacitors connected on VDD, VDDH, VDDL, EN, DT and BST should be placed as close to their respective pins as possible.
2) A not less than 100nF MLCC capacitor should be placed between VDDL and PGND. It should be placed as close to VDDL as possible.
3) A not less than 100nF MLCC capacitor should be placed between VDDH and SW. It should be placed as close to VDDH as possible.

4) High frequency switching current charges and discharges the gate and drain of GaN FETs, which causes EMI and ringing issues. The lengths of gate drive loop should be short to minimum the parasitic inductance and ringing affection.

5) The source and sink gate drive resistors should be placed as close to the GaN FETs as possible.

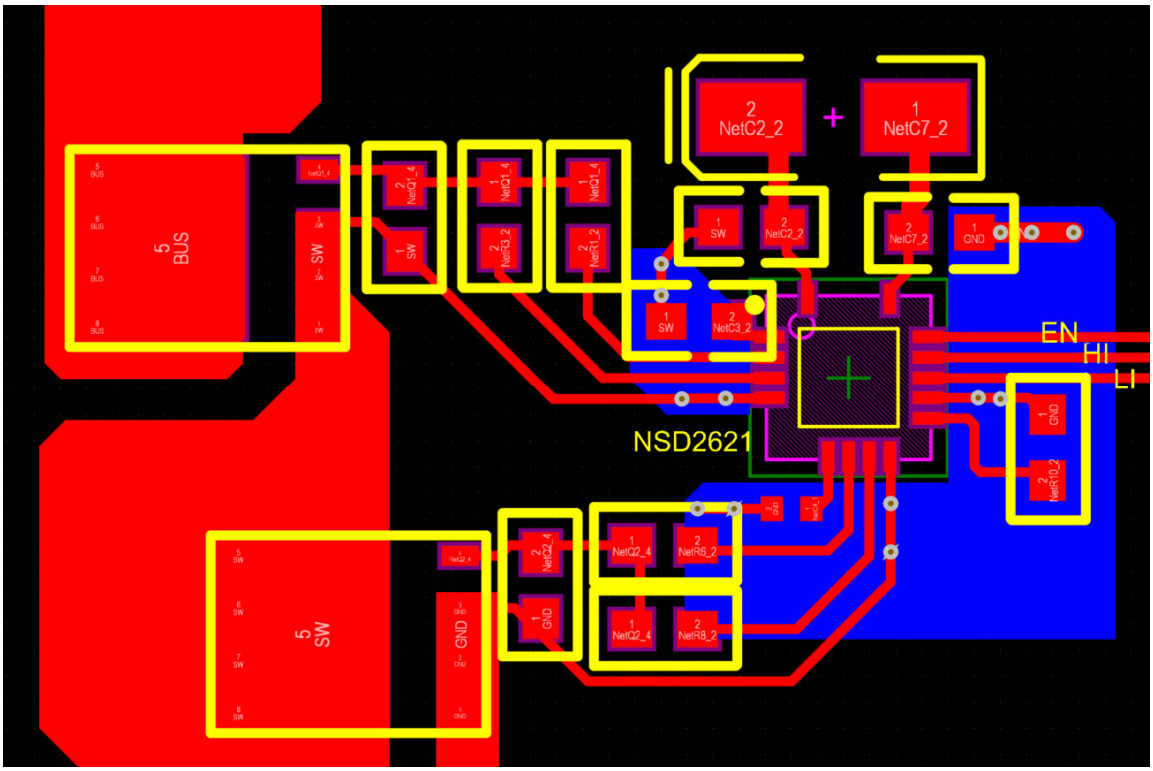
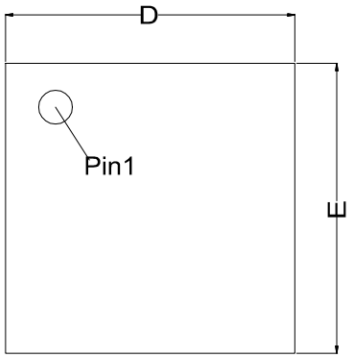


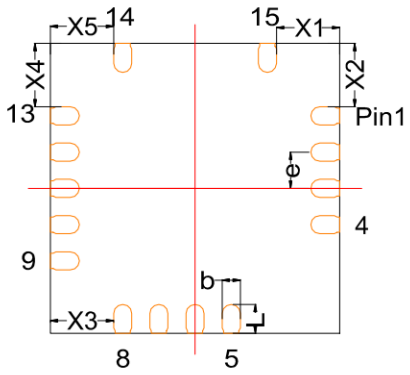
Figure. 8.2 PCB Layout Example

9. Package information

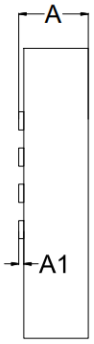
Package Top View



Package Bottom View



Package Side View



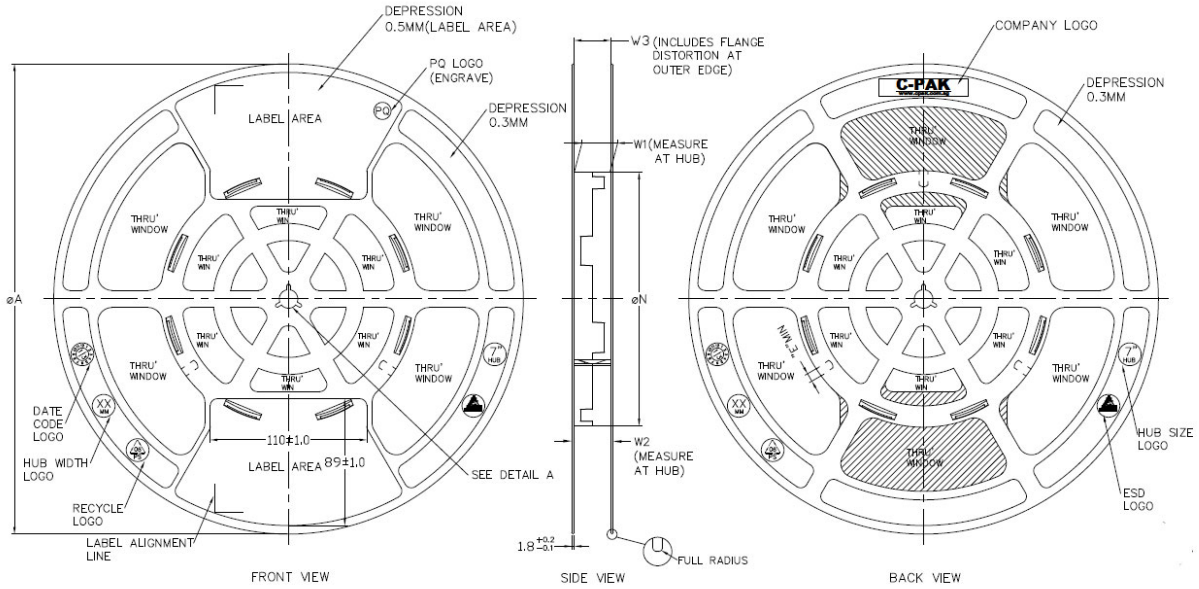
SYMBOLS	DIMENSION IN MM		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.007	0.012	0.017
D	3.900	4.000	4.100
E	3.900	4.000	4.100
e	0.450	0.500	0.550
b	0.200	0.250	0.300
L	0.350	0.400	0.450
X1	0.825	0.875	0.925
X2	0.825	0.875	0.925
X3	0.825	0.875	0.925
X4	0.825	0.875	0.925
X5	0.825	0.875	0.925

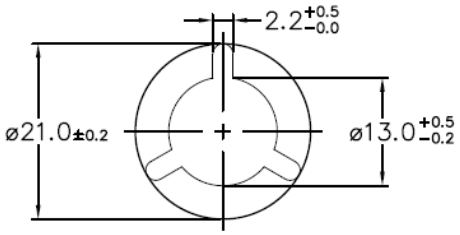
Figure. 9.1 Package Shape and Dimension

10. Ordering Information

Part No.	Temperature	Auto-motive	Package Type	MSL	SPQ
NSD2621A-DQAGR	-40 to 125°C	NO	QFN	3	4000
NSD2621C-DQAGR	-40 to 125°C	NO	QFN	3	4000

11. Tape and Reel Information





PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure. 11.1 Tape Information

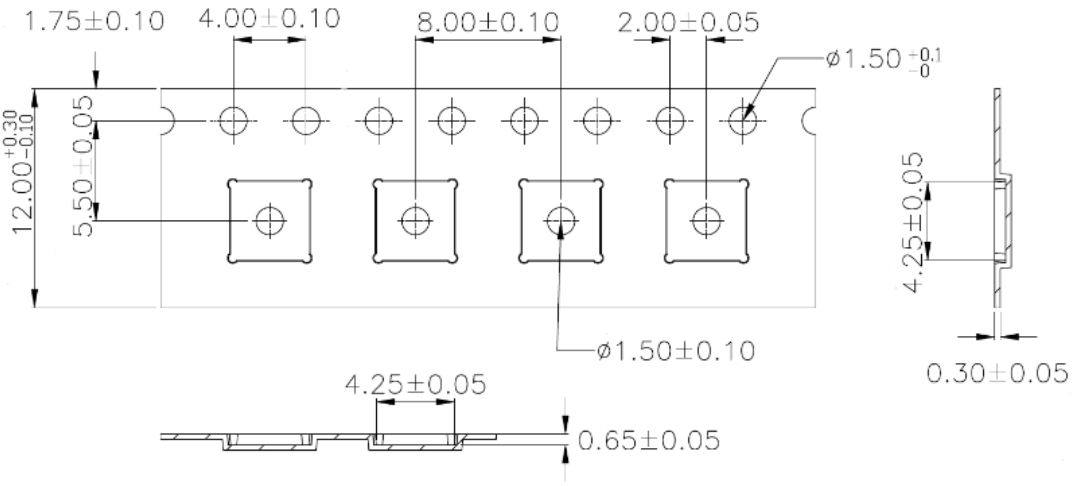


Figure. 11.2 Reel Information

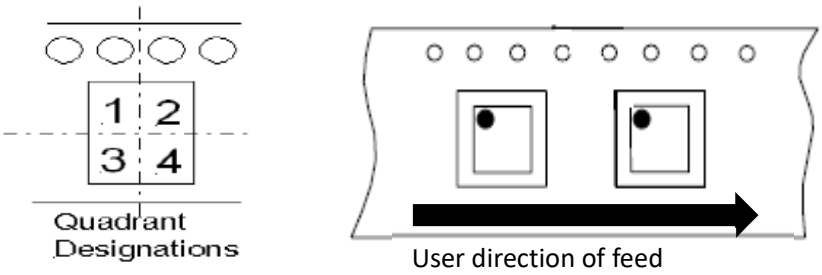


Figure. 11.3 Quadrant Designation for Pin1 Orientation in Tape

12. Revision History

Revision	Description	Date
1.0	Initial version	2023/12/27
1.1	Update the deadtime resistor configuration value.	2024/05/13
1.2	Update the SPQ from 2500 to 4000	2024/06/24

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

You are solely responsible for your use of Novosense' products and applications, and for the safety thereof. You shall comply with all laws, regulations and requirements related to Novosense's products and applications, although information or support related to any application may still be provided by Novosense.

The resources are intended only for skilled developers designing with Novosense' products. Novosense reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided. Novosense authorizes you to use these resources exclusively for the development of relevant applications designed to integrate Novosense's products. Using these resources for any other purpose, or any unauthorized reproduction or display of these resources is strictly prohibited. Novosense shall not be liable for any claims, damages, costs, losses or liabilities arising out of the use of these resources.

For further information on applications, products, and technologies, please contact Novosense (www.novosns.com).

Suzhou Novosense Microelectronics Co., Ltd